

COMPUTER ARCHITECTURE AND ORGANIZATION

Course Code	23EE4501C	Year	III	Semester	I
Course Category	PE-I	Branch	EEE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	NIL
Continuous Internal Evaluation:	30	Semester End Evaluation:	70	Total Marks:	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Explain the foundational principles of computer architecture and organization, including instruction cycles, processing units, memory, and I/O systems (L2)
CO2	Apply register transfer and microoperation techniques to interpret control logic and data flow in computer systems (L3)
CO3	Analyze pipelining and parallel processing mechanisms to evaluate their impact on processor performance (L4)
CO4	Apply interfacing techniques and memory system concepts to develop efficient communication between system components. (L3)
CO5	Prepare and submit a technical report demonstrating comprehensive understanding of computer architecture and organization

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3:High, 2: Medium, 1:Low)														
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1														
CO2	3												2	
CO3		3											2	
CO4	3												2	
CO5									3	3				

SYLLABUS		
Unit No.	Contents	Mapped CO
I	BASIC COMPUTER ORGANIZATION AND DESIGN Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input- Output and Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator Logic.	CO1 CO2 CO5
II	REGISTER TRANSFER AND MICRO OPERATIONS Register Transfer Language, Register Transfer, Bus and Memory Transfers,	CO1 CO2

	Arithmetic Micro operations, Logic Micro operations, Shift Micro operations, Arithmetic Logic Shift Unit. Micro programmed Control: Control Memory, Address Sequencing, Micro program Example, Design of Control Unit	CO5
III	CENTRAL PROCESSING UNIT Introduction, General Register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer (RISC) Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors.	CO1 CO3 CO5
IV	INPUT/OUTPUT ORGANIZATION Peripheral Devices, I/O interface, Asynchronous data transfer, Modes of transfer, priority Interrupt, Direct memory access, Input-Output Processor (IOP), Serial Communication.	CO1 CO4 CO5
V	MEMORY ORGANIZATION Memory Hierarchy, Main memory, Auxiliary memory, Associate Memory, Cache Memory, and Virtual memory, Memory Management Hardware.	CO1 CO4 CO5

Learning Resources	
Textbooks:	
1. M. Morris Mano, “Computer System Architecture”, Prentice Hall of India Pvt. Ltd., 3 rd Edition, Sept. 2008	
Reference Books:	
1. William Stallings, “Computer Architecture and Organization”, PHI Pvt. Ltd., Eastern Economy Edition, Sixth Edition, 2003.	
2. Linda Null, Julia Lobur, “Computer Organization and Architecture”, Narosa Publications.	
3. John. P. Hayes , “Computer System Organization”, Mc GrawHill, 3 rd edition, 2017.	