Digital System Design through HDL

Course Code	23EC4501A	Year	III	Semester	I
Course Category	PE -I	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Pre requisites	STLD
Continuous Internal Evaluation	30	Semester End Evaluation	70	Total Marks	100

Course Outcomes		
Upon successful completion of the course, the student will be able to		BL
CO1	Understand the language constructs and programming fundamentals of Verilog HDL	L2
CO2	Choose the suitable abstraction level for a particular digital design.	L2
CO3	Construct Combinational and sequential circuits in different modelling styles using Verilog HDL	L4
CO4	Design and synthesize combinational and sequential logic circuits	L4
CO5	Analyze and Verify the functionality of digital circuits/systems using test benches.	L4

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of Correlations (3:High, 2:Medium, 1:Low)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2				2							1	2	
CO2	2				2							1	2	
CO3	3	3			2							1	3	
CO4	3	3			2							1	3	
CO5	3	3			2							1	3	
Avg.	3	3			2							1	3	

Syllabus

Unit No.	Contents	Mapped CO
1	**Introduction to Verilog HDL and Gate Level Modelling:** Verilog as HDL, Levels of Design Description Basics of Concepts of Verilog, Data Types, System Task, Compiler directives, modules and ports. AND Gate Primitive, Module Structure, Other Gate Primitives	CO1
2	**Modelling at Behavioural Modelling:** Introduction, structured processors, procedural assignments, timing controls, conditional statements, multi-way branching, loops, sequential and parallel blocks, generate blocks, Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in Behavioral model..	CO2, CO3
3	**Modelling at Data flow Level:** Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators, Design of Decoders, Multiplexers, Switch Level Modelling: Introduction, Basic Transistor Switches, CMOS Switch.	CO2, CO3,
4	**FSM Design:** Functions, Tasks, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines), Encoding Style: From Binary to One Hot. Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic.	CO4

5	**Components Test and Verification:** Test Bench – Combinational Circuits Testing, Sequential Circuits Testing, Test bench Verification flow, Examples using Verilog HDL.	CO5

Learning Resources
Text Books
1. Palnitkar, "Verilog HDL A Guide to Digital and Synthesis" ,2nd Ed., Pearson Education. 2. Michael, D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson Education India
Reference Books
1. Padmanabhan, Tripura Sundari , Design through Verilog HDL, Wiley Publications. 2. S. Brown, Zvonko – Vranesic, Fundamentals of Digital Logic with Verilog Design, TMH, 3. J. Bhasker, A Verilog HDL Primer 2nd Ed., BS Publications.
e- Resources & other digital material
1. https://archive.nptel.ac.in/courses/106/105/106105165/