PVP 23

Code: 23EC3501

III B.Tech - I Semester - Regular Examinations - NOVEMBER 2025

ANALOG AND DIGITAL IC APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

PART – A

		BL	CO
1.a)	Define ideal op-amp.	L2	CO1
1.b)	List two applications of op-amp.	L2	CO1
1.c)	Define CMRR of op-amp.	L2	CO5
1.d)	Write two advantages of active filters over passive filters.	L2	CO1
1.e)	Write the different types of ADC and DAC.	L2	CO3
1.f)	Write the function of IC555 in monostable mode.	L2	CO2
1.g)	Define multiplexer.	L2	CO4
1.h)	Give one application of a Schmitt Trigger.	L2	CO5
1.i)	Write the difference between Static and Dynamic RAM.	L2	CO4
1.j)	Write the purpose of EPROM.	L2	CO4

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	List in detail the DC & AC characteristics of Op-Amp.	L2	CO5	4 M
	b)	Analyze the subtractor amplifier and derive the expression for output.	L4	CO5	6 M
		OR			
3	a)	Design an Op-Amp circuit to produce an output voltage that is proportional to the derivative of the input voltage with neat circuit and output diagrams.	L3	CO5	5 M
	b)	Design a comparator circuit using an Op-Amp. Explain how the output changes for an input signal.	L3	CO5	5 M
		UNIT-II			
4	a)	Design first order High Pass Filter for cutoff frequency of 10 KHz.	L3	CO5	5 M
	b)	Design the Square Wave Generator for frequency of 10KHz by assuming necessary data.	L3	CO5	5 M
		OR			
5	a)	Design first order Low Pass Filter for cutoff frequency of 1 KHz.	L3	CO2	5 M
	b)	Design a monostable multivibrator using IC 555 to generate a pulse width of 2 ms	L3	CO2	5 M

		when triggered by an external input. Assume a supply voltage of 5 V and choose suitable values of resistor and capacitor. Draw the circuit diagram and explain the working.			
		UNIT-III			
6	a)	Demonstrate the operation of Counter Type ADC with circuit diagram.	L3	CO3	5 M
	b)	Design and explain the operation of a Dual Slope ADC for converting Analog to Digital.	L3	CO3	5 M
		OR			
7	a)	Demonstrate the operation of Weighted Resistor DAC with circuit diagram.	L3	CO3	6 M
	b)	Discuss the key specifications of DAC and ADC.	L2	CO3	4 M
		UNIT-IV			
8	a)	Demonstrate the logic symbol and function table of comparator IC 7485.	L3	CO4	5 M
	b)	Explain the operation of the BCD-to-7-segment code converter with function table.	L2	CO4	5 M
		OR			
9	a)	Realize 32:1 Multiplexer using 74151 ICs.	L3	CO4	5 M
	b)	Design a circuit to perform 8-bit binary addition using two 4 bit adder IC 7483s connected in cascade.	L3	CO4	5 M

		UNIT-V			
10	a)	Discuss in detail about the differences between a latches and a flip-flops.	L2	CO4	4 M
	b)	Explain the architecture of Random Access Memory (RAM). Highlight the differences between Static RAM and Dynamic RAM.	L2	CO4	6 M
		OR			
11	a)	Discuss the Principle of operation of ROM.	L2	CO1	5 M
	b)	Design and explain the working of a decade counter using IC 7490. Draw its internal block diagram and truth table.	L3	CO1	5 M

PVP SIDDHARTHA INSTITUTE OF TECHNOLOGY
(AUTONOMOUS)

111 B.Tech - 1 Semester - Regular Examinations - NOVEMBER 2025

ANALOG AND DIGITAL IC APPLICATIONS

(ELECTRONICS & COMMUNICATION ENGINEERING)

Q.NO		Marks Distribution	Total Marks
1	a	Definition	2
1	b	Each application -1M	2
1	c	Definition	2
1	d	Each advantage -1M	2
1	e	ADC types-1M DAC types -1M	2
1	f	Definition	2
1	g	Definition	2
1	h	Any application	2
1	i	Each difference-1M	2
1	j	Any purpose	2
2	a	DC Characteristics of op-amp = 2M AC characteristics of Op-Amp=2M	4
	b	Circuit diagram-3M Derivation-3M	6
3	a	Circuit diagram-2M Derivation-3M	5
	b	Circuit diagram-2M Explanation=3M	5
4	a	Circuit diagram-2M Calculation-3M	5
	b	Circuit diagram-2M Calculation-3M	5
5	a	Circuit diagram-2M Calculation-3M	5
	b	Circuit diagram-2M Calculation-3M	5
6	a	Circuit diagram-2M Explanation=3M	5
	b	Circuit diagram-2M Explanation=3M	5

7	a	Circuit diagram-2M Explanation=4M	6
	b	Each specification 1M	4
8	a	Pin diagram-2M Explanation=3M	5
	b	Diagrams-2M Explanation-3M	5
9	a	Circuit diagram-5M	5
	b	Circuit diagram-5M	5
10	a	Each difference -2M	4
	b	Principle of RAM-4M Key difference-2M	6
11	a	Principle of ROM-3M Diagram-2M	5
	b	Diagrams-2M Explanation-3M	5

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ANALOG AND DIGITAL IC APPLICATIONS

(ELECTRONICS & COMMUNICATION ENGINEERING)

PART-A

1.(a) Define ideal op-amp

Ideal OP Amp Definition: An ideal OP Amp is defined as a differential amplifier with infinite open loop gain, infinite input resistance, Infinite Bandwidth , zero output resistance and Zero Offset Voltage.

1.(b) List two applications of op-amp

Any two of the following

The applications of the op-amp are:

op amp as signal amplifier

op amp as filters

op amp as voltage comparators

op amp as oscillators

op amp as differentiator

op amp as integrator

op amp as voltage to current converter

op amp as current to voltage converter

op amp as logarithmic amplifier

op amp as half wave rectifier

op amp as non-inverting amplifiers

op amp as inverting amplifiers

op amp as phase shifter

op amp as adder or summing amplifier

1.(c) Define CMRR of op-amp.

CMRR (Common mode rejection ratio) is defined as the ratio of differential-mode voltage gain (Ad) and the common-mode voltage gain (Ac).

1.(d) Write two advantages of active filters over passive filters.

Signal Amplification and Power Gain Capability

Active filtering doesn't require bulky magnetic parts like coils or transformers, so engineers can build much smaller circuits that still perform really well in practice.

1.(e) Write the different types of ADC and DAC.

types of ADCs in use today:

Successive Approximation (SAR) ADC

Counter type ADC

Dual Slope ADC

Flash ADC

DAC:

Binary-Weighted DAC

Uses resistors weighted in powers of two.

R-2R Ladder DAC

Uses a resistor ladder network with only two resistor values (R and 2R).

1.(f) Write the function of IC555 in monostable mode.

555 monostable circuit can generate pulses from a few microseconds to several seconds depending on the values of resistor R and capacitor C.

1(g) Define multiplexer

A multiplexer is a combinational circuit that has many data inputs and a single output, depending on control or select inputs.

1(h) Give one application of a Schmitt Trigger

Schmitt trigger is a comparator circuit that makes use of positive feedback to implement hysteresis and is used to remove noise from an analog signal while converting it to a digital one.

1(i) Write the difference between Static and Dynamic RAM.

SRAM	DRAM
It stores information as long as the power is supplied.	It stores information as long as the power is supplied or a few milliseconds when the power is switched off.
Transistors are used to store information in SRAM.	Capacitors are used to store data in DRAM.
Capacitors are not used hence no refreshing is required.	To store information for a longer time, the contents of the capacitor need to be refreshed periodically.
SRAM is faster compared to DRAM.	DRAM provides slow access speeds.

1(j) Write the purpose of EPROM

EPROM stands for Erasable Programmable Read-Only Memory is a kind of non-volatile memory used in computers and other electronic devices for storing data that must be retained even when the power is turned off.

It can be reused again and again as it is easily programmable and erasable. A chip that uses ultraviolet (UV) light to erase data is called an EPROM.

PART-B

2(a) List in detail the DC & AC characteristics of Op-Amp.

DC Characteristics of op-amp:

1. **Input bias current**
2. **Input offset current**
3. **Input offset voltage**
4. **Thermal drift**

Input offset voltage

Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output as shown in Fig.. In figure V_{dc1} and V_{dc2} are dc voltages and R_S represents the source resistance. We denote input offset voltage by V_{io}. This voltage V_{io} could be positive or negative. For a 741C, the maximum value of V_{io} is 6mV dc. The smaller the value of V_{io}, the better the input terminals are matched. For instance, the 741C precision op-amps has maximum V_{io}= 150μV.

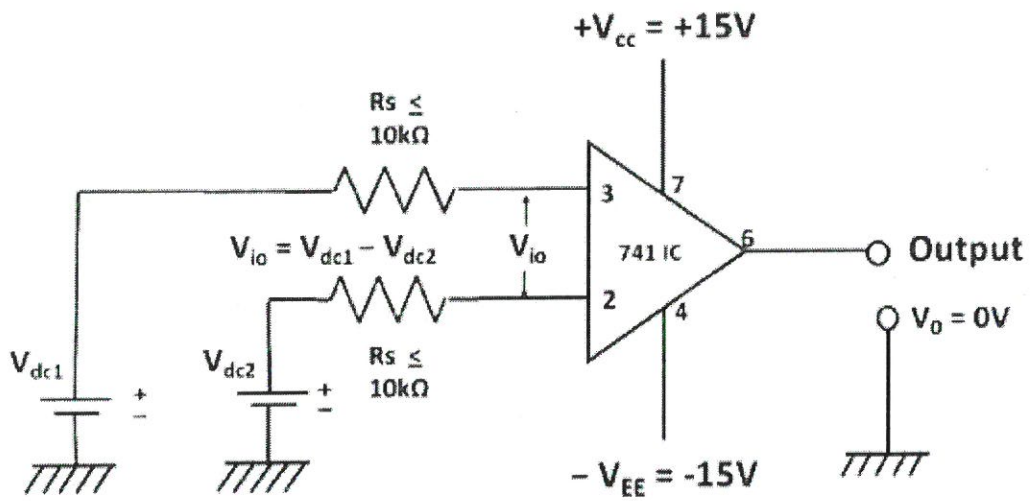


Fig-: Input offset voltage V_{io}

Input offset current

The algebraic difference between the currents into the inverting and non-inverting terminals is known as input offset current I_{io}(Fig.). In the form of an equation,

$$I_{io} = |I_{B1} - I_{B2}|$$

where I_{B1} is the current into the non-inverting input and I_{B2} is the current into the inverting input. The input offset current for the 741C is maximum 200nA . As the matching between two

input terminals is improved, the difference between $I_{B1}$and I_{B2} becomes smaller; i.e. the I_{io} value decreases further. For instance, the precision op-amp 741C has a maximum value of lio equal to 6nA, a dramatic improvement over older technology.

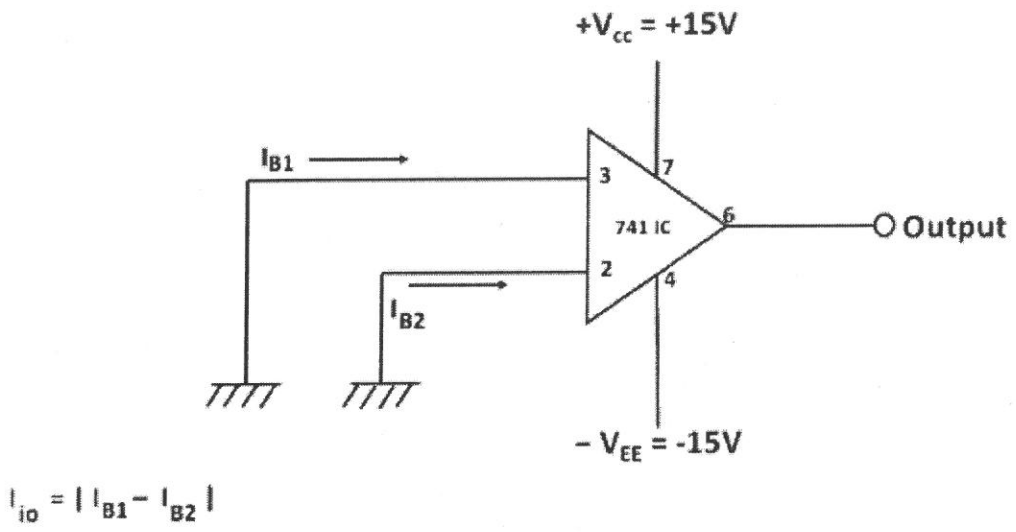


Fig: Input offset current I_{io}

Input bias current

Input bias current I_B, is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp. In the form of an equation,

$$I_B = (I_{B1} + I_{B2})/2$$

I_B = 500nA (maximum) for 741C, whereas for the precision 741C, it is ±7nA. The two input currents I_{B1} and I_{B2} are actually the base currents of the first differential amplifier stage.

Thermal drift:

- Bias current, offset current, and offset voltage change with temperature.
- A circuit carefully nulled at 25°C may not remain. So when the temperature rises to 35°C. This is called drift.

AC Characteristics of Op-Amps

AC characteristics relate to the behavior of the op-amp with time-varying (alternating) input signals.

1. **Gain-Bandwidth Product (GBW or GBP):**
   - The product of the amplifier's bandwidth and its gain is constant.
   - Indicates that higher gain reduces bandwidth and vice versa.
2. **Slew Rate (SR):**

- The maximum rate of change of the output voltage per unit time, typically in V/μs.
- Limits the speed of the output signal change.

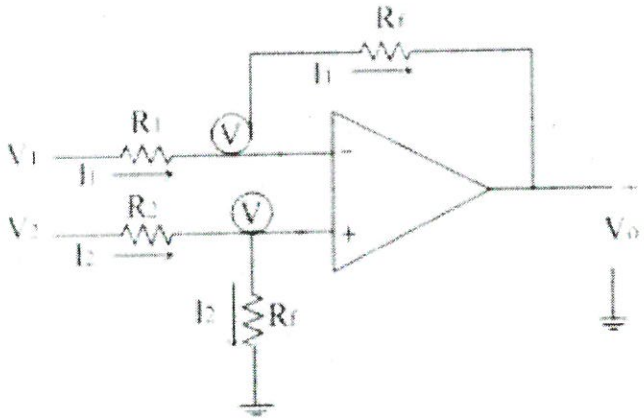
3. **Frequency Response:**
   - Shows how gain decreases with increasing frequency.
   - .
4. **Phase Margin and Stability:**
   - Phase shift at unity gain frequency affects stability.
   - Important for designing feedback circuits to avoid oscillations.

2. (b) Analyze the subtractor amplifier and derive the expression for output.

Subtractor/Difference Amplifier

A basic differential amplifier can be used as a subtractor when input signals are applied at the two input terminals of op-amp i.e. one at inverting and other at non-inverting terminal, then output is given by the difference of two input signals. The practical circuit of the op-amp as subtractor is given in Fig.. It is a combination of inverting and non-inverting amplifiers.

The subtraction of the two input voltages is possible with the help of subtractor. The subtractor using op-amp is shown in figure below. It is also called as difference amplifier.



The input signals applied are V1 and V2.
Let us assume that the non-inverting terminal is at potential 'V'. Due to virtual ground concept, the inverting terminal appears to be at the same potential 'V' as shown in the circuit diagram.

Let the current flowing through resistance R1 and R2 are I1 and I2 respectively. Since input current to the op-amp is zero, the two currents flows through the resistance Rf as shown in circuit diagram above. The current I2 is given as

$$I_2 = \left[\frac{V_2 - V}{R_2}\right] = \left[\frac{V - 0}{R_f}\right]$$

From the above equation voltage 'V' can be calculated as

$$\frac{V_2}{R_2} - \frac{V}{R_2} = \frac{V}{R_f}$$

$$\therefore \quad \frac{V_2}{R_2} = \frac{V}{R_2} + \frac{V}{R_f}$$

$$\therefore \quad \frac{V_2}{R_2} = V\left[\frac{R_2+R_f}{R_2R_f}\right]$$

$$\therefore \quad V = V_2\left[\frac{R_f}{R_2+R_f}\right]$$

The current I1 is given as

$$I_1 = \frac{V_1-V}{R_1} = \frac{V-V_o}{R_f}$$

Simplify the equation,

$$\frac{V_1}{R_1} - \frac{V}{R_1} = \frac{V}{R_f} - \frac{V_o}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V}{R_f} + \frac{V}{R_1} - \frac{V_1}{R_1}$$

$$\frac{V_o}{R_f} = V\left[\frac{R_f+R_1}{R_fR_1}\right] - \frac{V_1}{R_1}$$

Substituting the voltage 'V' from the equation we get,

$$\frac{V_o}{R_f} = V_2\left(\frac{R_f}{R_f+R_2}\right)\left[\frac{R_f+R_1}{R_fR_1}\right] - \frac{V_1}{R_1}$$

$$V_o = V_2\left(\frac{R_f}{R_f+R_2}\right)\left[\frac{R_f+R_1}{R_1}\right] - \frac{R_fV_1}{R_1}$$

If R1=R2

$$V_o = \frac{R_f}{R_1}[V_2 - V_1]$$

If R1=R2=Rf

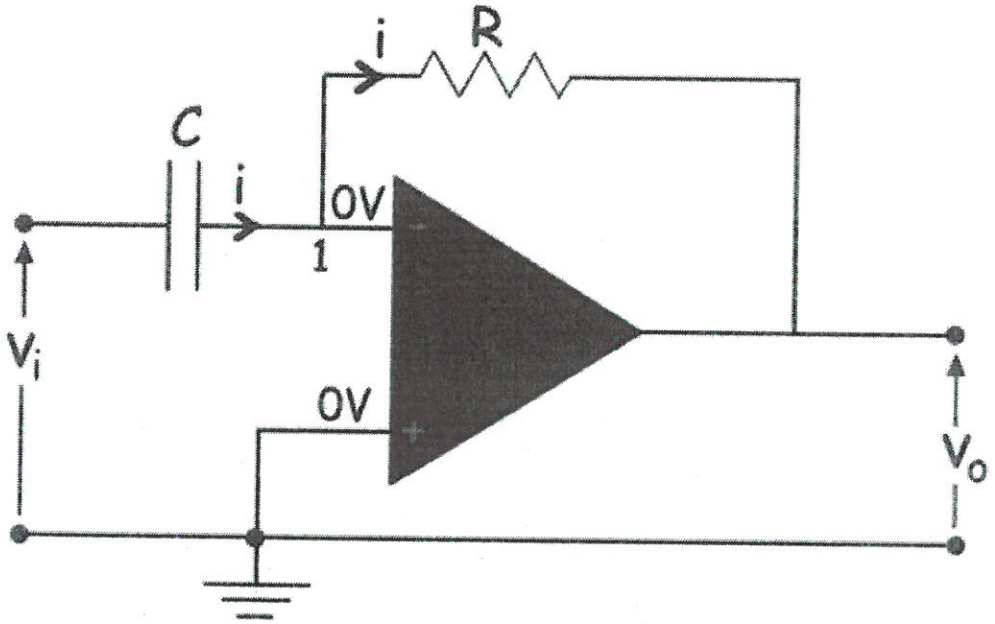
$$V_o = [V_2 - V_1]$$

Thus at the output we get subtraction of the two input voltages.

3(a) Design an Op-Amp circuit to produce an output voltage that is proportional to the derivative of the input voltage with neat circuit and output diagrams.

The differentiator amplifier circuit produces an output voltage signal which is the time derivative of the input signal

An **op amp differentiator** is an inverting amplifier with a capacitor at the input terminal. The basic circuit diagram illustrates this setup.



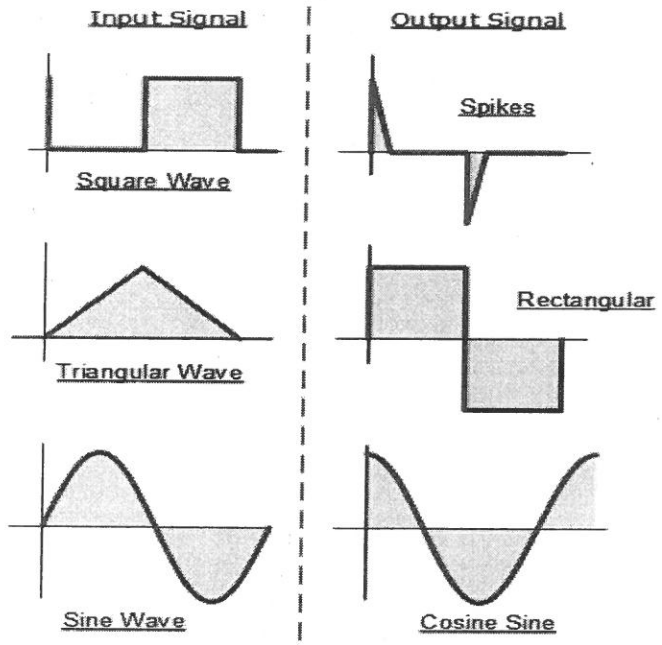
We will first assume that the op amp used here is an ideal op amp. We know that the voltage at both inverting and non inverting terminals of an ideal op amp is same. As the electric potential at non inverting terminal is zero since it is grounded. The electric potential of inverting terminal is also zero, as the op_amp is ideal. Because, we know that the electric potential at non – inverting and inverting terminals. It is also known to us that the current entering through inverting and non inverting terminal of an ideal op amp is zero.
Given these ideal op amp conditions, applying Kirchhoff Current Law at node 1 of the op amp differentiator circuit, we find:

$$C\frac{dv_i}{dt} = -\frac{v_0}{R}$$

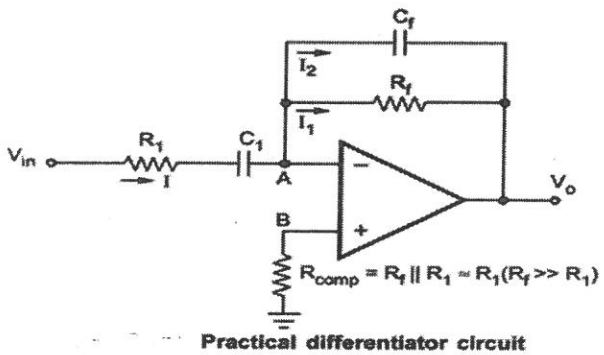
$$\Rightarrow v_0 = -RC\frac{dv_i}{dt}$$

This equation indicates that the output voltage is the derivative of the input voltage.

Op-amp Differentiator Waveforms



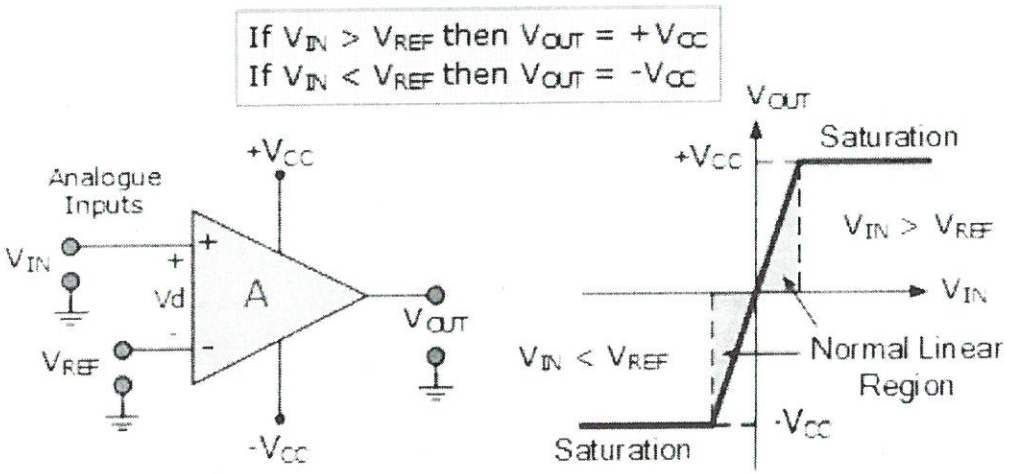
Improved Op-amp Differentiator



Practical differentiator circuit

3(b) Design a comparator circuit using an OpAmp. Explain how the output changes for an input signal

Voltage Comparator Circuit



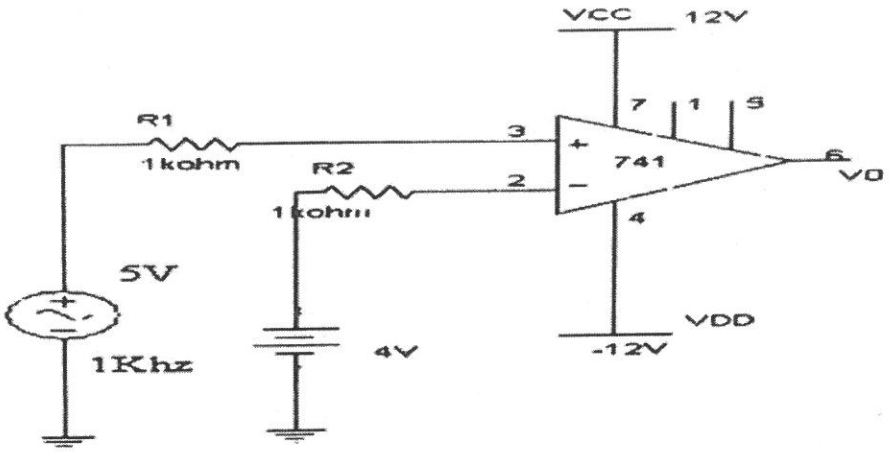
The Op-amp comparator compares one analogue input voltage level with another analogue input voltage level, or some pre-set reference voltage, VREF and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two input voltages and determines which is the largest of the two.

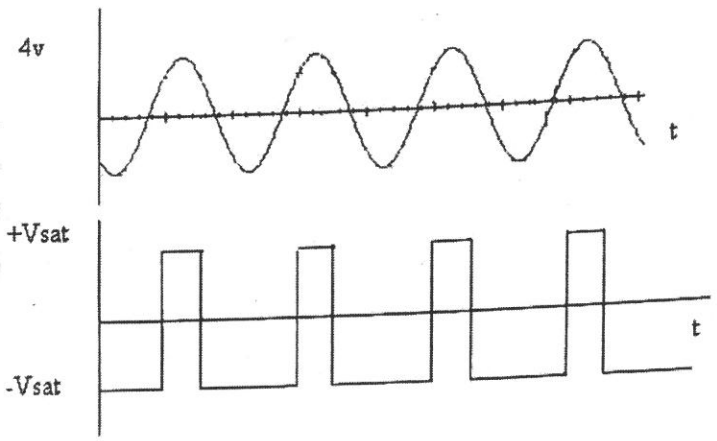
Then due to this high open loop gain, the output from the comparator swings either fully to its positive supply rail, +Vcc or fully to its negative supply rail, -Vcc on the application of varying input signal which passes some preset threshold value.

The open-loop op-amp comparator is an analogue circuit that operates in its non-linear region. Changes in its two analogue inputs, V+ and V- causes it to behave much like a digital bistable device, since triggering causes it to have two possible output states, +Vcc or -Vcc.

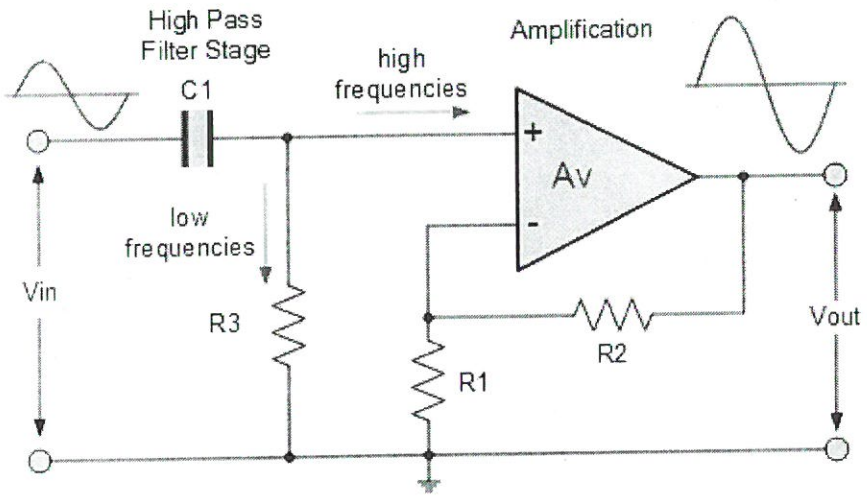
Then we can say that the voltage comparator is essentially a 1-bit analogue to digital converter, as the input signal is analogue but the output behaves digitally.

Comparator with sin wave at the input is shown below.


VCC
12V
R1
1kohm
R2
1kohm
3
2
7
1
8
741
6
VO
4
5V
1Khz
4V
VDD
-12V


4v
t
+Vsat
-Vsat
t

4(a) Design first order High Pass Filter for cutoff frequency of 10 KHz



cut-off frequency (fc) can be found by using the same formula:

filter cut-off frequency

$$fc = \frac{1}{2\pi RC}\ Hz$$

the pass-band gain of the filter, AF assume

$$A_F = 1 + \frac{R_2}{R_1}, \quad \therefore 2 = 1 + \frac{R_2}{R_1} \quad \text{and} \quad \frac{R_2}{R_1} = 1$$

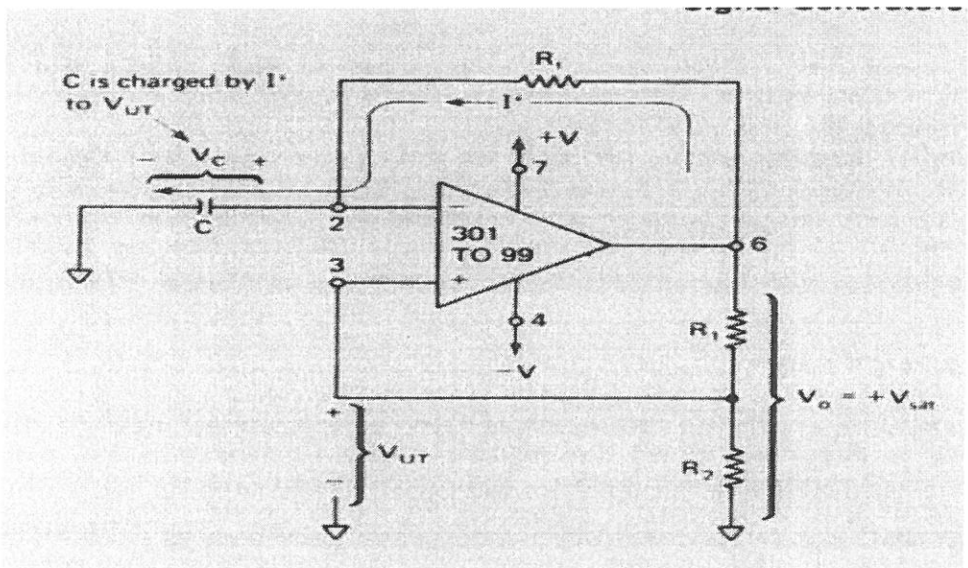
Assume capacitor value,

the value of R will therefore be:

$$R = \frac{1}{2\pi f_C C}$$

4(b)Design the Square Wave Generator for frequency of lOKHz by assuming necessary data

using op_amp
Astable multi vibrator



Total time period

$$T = 2T_1 = 2RC\ln\frac{1+\beta}{1-\beta} \qquad (5.8)$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC$ ln 3. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\ RC$

f=10KHZ
T-1/ f where f-frequency

Assume C value like 0.1uf or 0.01 uf or any suitable value

Calculate R value using above formula

Or
Assume R any suitable value

Calculate C value using above formula

Using IC 555 astable

$$t_{HIGH} = 0.69\ R_A C$$

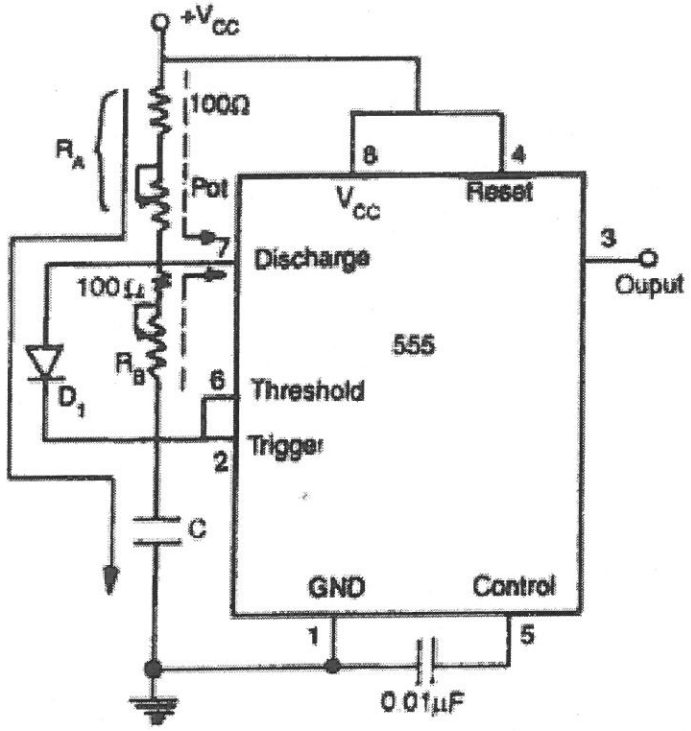


Fig. 8.19 Adjustable duty cycle rectangular wave generator

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $$t_{LOW} = 0.69\ R_B C \tag{8.15}$$

$$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C \tag{8.16}$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \tag{8.17}$$

If diode is not inserted

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or,
$$T = 0.69\ (R_A + 2R_B)\ C$$

So,
$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \qquad (8.13)$$

Assume Resistor values equal
or $R_A = KR_B$ K=1,2,3,4 ....

Assume C value 0.1 uf or 0.01uf or any suitable value

Calulate Resistor values

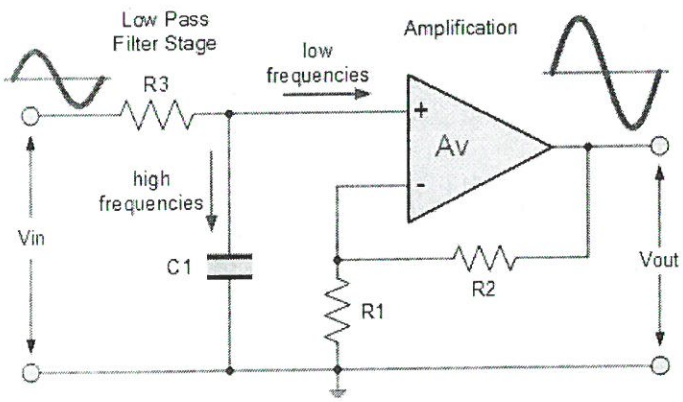
Or

Assume resistor values like 10K Ω,

Calculate C value

5(a) Design first order Low Pass Filter for cutoff frequency of 1 KHz

Active Low Pass Filter with Amplification
first order active low pass filter



Assume A_F= any value

$$A_F = 1 + \frac{R_2}{R_1} = 10$$

Assume a value for resistor R1 of 1kΩ rearranging the formula above gives a value for R2 of:

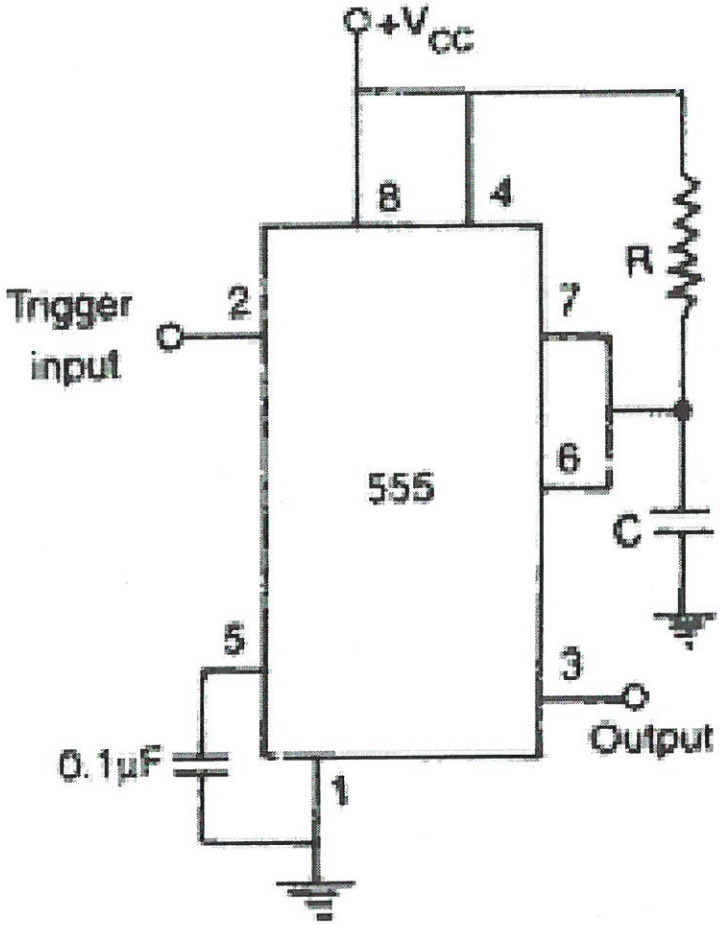
$$R_2 = (10 - 1)\ x\ R_1 = 9\ x\ 1k\Omega = 9k\Omega$$

Assume capacitor value,

the value of R will therefore be:

$$R = \frac{1}{2\pi f_c C}$$

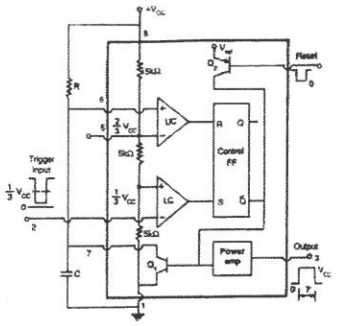
5(b) Design a monostable multivibrator using IC 555 to generate a pulse width of 2 ms. Draw the circuit diagram and explain the working



One of the most versatile linear ICs is the 555 times. The 555 is a monolithic timing circuit that can produce highly stable time delays or oscillation. The timer basically operates in one of the two modes either as monostable or as an astable multivibrator.

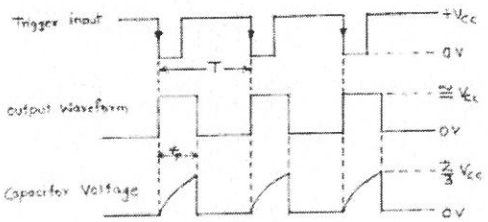
A monostable multivibrator, often called a one-shot multivibrator, is a Pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state the output of the circuit is approximately zero or at logic-low level. When an external trigger pulse is applied, the output is forced to go high (≅ Vcc). The time the output remains high is determined by the external RC network connected to the timer. AT the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output remains low until the trigger pulse is again applied. Then the cycle

repeats. The monostable circuit has only one stable state (output low), hence the name monostable. Normally, the output of the monostable multivibrator is low



Monostable operation:

According to Figure 1 initially when output is low, that is , the circuit is in a stable state, transistor Q1 is on and the capacitor C is shorted out of the ground. However, upon application of a negative trigger pulse to pin 2, transistor Q1 is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up toward V_{CC} through R_A. However, when the voltage across the capacitor equals 2/3 V_{CC}, comparator 1's output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q1 ON, and hence capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Figure shows the trigger input, output voltage, and capacitor voltage waveform. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 V_{CC}.



$$T = 1.1\ RC\ \text{(seconds)}$$

T=2ms

Assume C value like 0.1uf
Calculate R value

6(a) Demonstrate the operation of Counter Type ADC with circuit diagram

In nature most of the signal around us is analog in nature i.e. all changes and physical phenomenon occurring are continuous. However due to the various advantages of having data in digital format like storage, processing, transmission etc., we prefer to convert these continuous varying quantities into discreet digital values. This process in known as quantization and the device employed for quantization is known as an Analog to Digital Converter – ADC.

Most ADC's use a circuit called a comparator. The circuit has two inputs and one output. Inputs are the analog signals & output is a single bit digital signal.

ADCs convert voltages that represent real-world signals into bits that microprocessors and software use to manipulate test data and control test equipment. Even if you work on digital signals exclusively, you probably use an ADC in an oscilloscope to look at the analog characteristics of your signals.

One of the simplest types of the ADC is the Counter type ADC. The input signal of the ADC is connected to the signal input of its internal comparator. ADC then systematically increases the voltage on the reference input of the comparator until the reference becomes larger than the signal & the comparator output goes to zero.

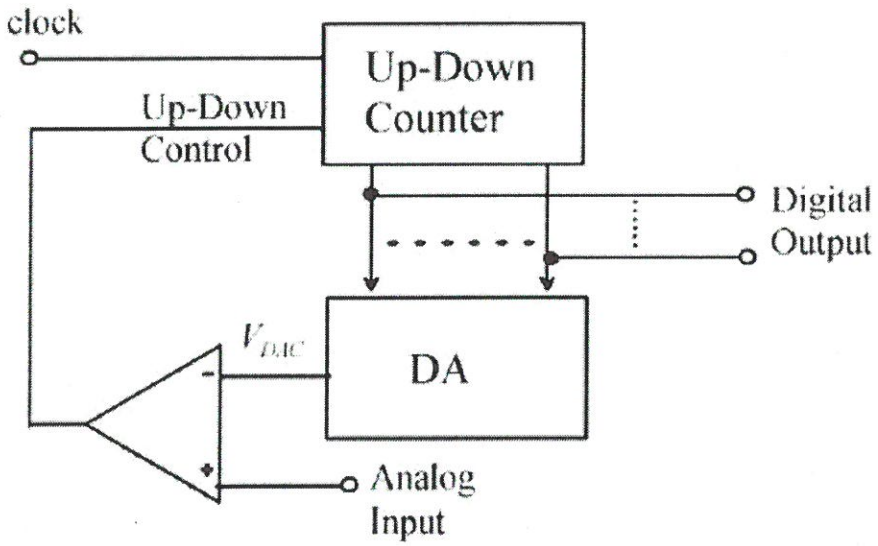
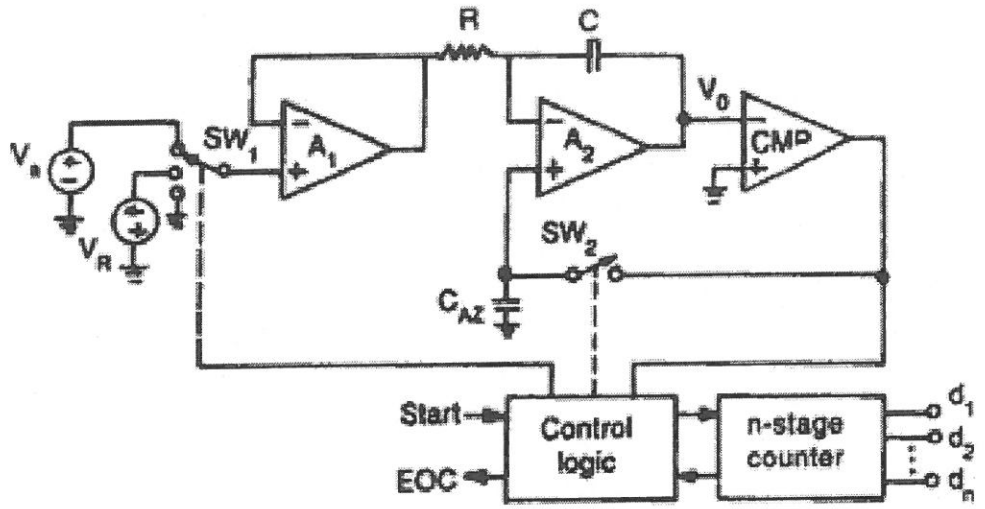
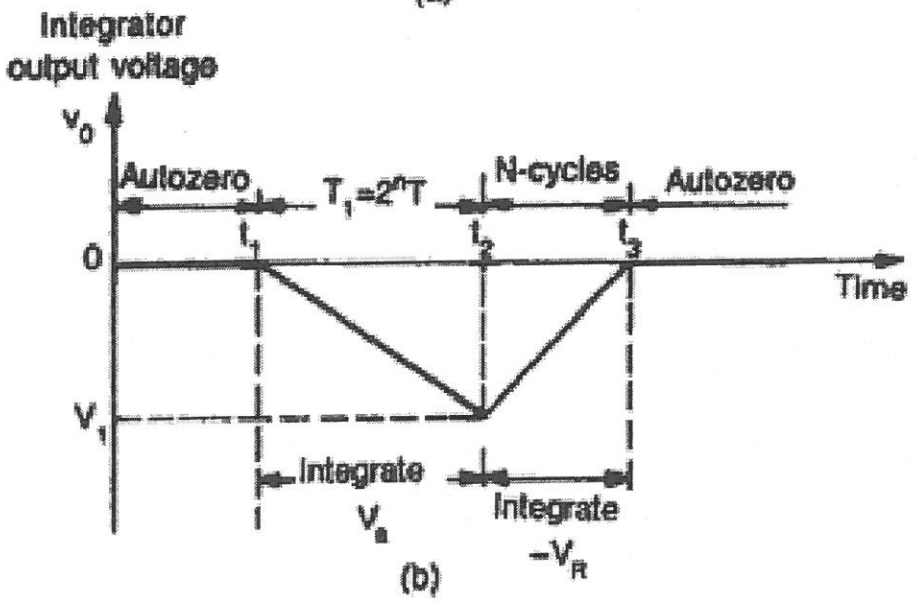


Fig.1 Counter type ADC

6(b) Design and explain the operation of a Dual Slope ADC for converting Analog to Digital.



(a)



(b)

Operation:
The binary counter is initially reset to 0000; the output of integrator reset to 0V and the input to the ramp generator or integrator is switched to the unknown analog input voltage VA.

The analog input voltage VA is integrated by the inverting integrator and generates a negative ramp output. The output of comparator is positive and the clock is passed through the AND gate. This results in counting up of the binary counter.

The negative ramp continues for a fixed time period t1, which is determined by a count detector for the time period t1. At the end of the fixed time period t1,

When the counter reaches the fixed count at time period t1, the binary counter resets to 0000 and switches the integrator input to a negative reference voltage –Vref.
Now the ramp generator starts with the initial value –Vs and increases in positive direction until it reaches 0V and the counter gets advanced. When Vs reaches 0V, comparator output becomes negative (i.e. logic 0) and the AND gate is deactivated. Hence no further clock is applied through AND gate. Now, the conversion cycle is said to be completed.

The voltage v_o will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\ V_a(t_2 - t_1)$$

The voltage v_1 is also given by

$$v_1 = (-1/RC)\ (-V_R)\ (t_2 - t_3)$$

So,
$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

7(a) Demonstrate the operation of Weighted Resistor DAC with circuit diagram

Weighted Resistor DAC

A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using binary weighted resistors in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC. The circuit diagram of a 3-bit binary weighted resistor DAC is shown in the following figure -

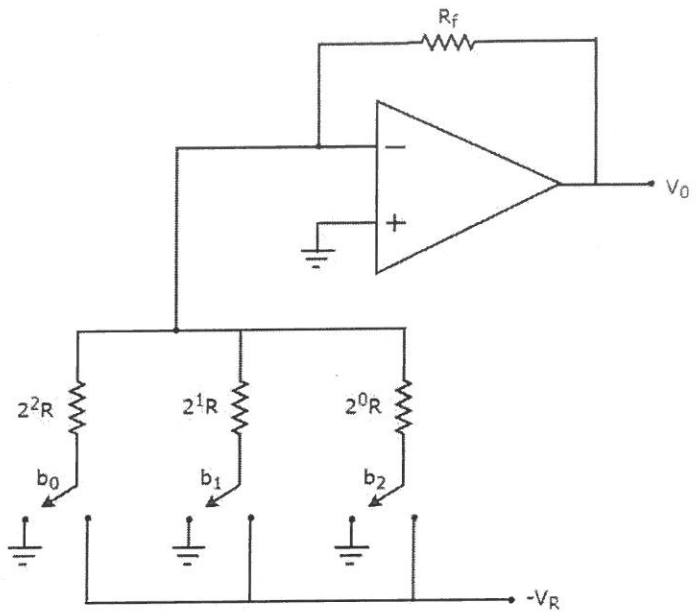


Figure 2

The bits of a binary number can have only one of the two values. i.e., either 0 or 1. Let the 3-bit binary input is $b_2b_1b_0$. Here, the bits b_2 and b_0 denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively. The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage, −VR when the corresponding input bits are equal to '1'. In the above circuit, the non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp. According to the virtual short concept, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

$$\frac{0+V_Rb_2}{2^0R}+\frac{0+V_Rb_1}{2^1R}+\frac{0+V_Rb_0}{2^2R}+\frac{0-V_o}{R_f}=0$$

$$\frac{V_o}{R_f}=\frac{V_Rb_2}{2^0R}+\frac{V_Rb_1}{2^1R}+\frac{V_Rb_0}{2^2R}$$

$$V_o=\frac{V_RR_f}{R}(\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2})$$

The above equation represents the output voltage equation of a 3-bit binary weighted resistor DAC. Since the number of bits are three in the binary (digital) input, we will get seven possible values of output voltage by varying the binary input from 000 to 111 for a fixed reference voltage, VR. We can write the generalized output voltage equation of an N-bit binary weighted resistor DAC as shown below based on the output voltage equation of a 3-bit binary weighted resistor DAC.

$$V_o = I_o R_f = V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

7(b) Discuss the key specifications of DAC and ADC

Key Parameters of ADCs

Resolution

Definition

The smallest difference in the analog input signal that an Analog-to-Digital Converter (ADC) can detect is referred to as resolution in this context. In essence, it refers to how many distinct levels the ADC can represent. An ADC with a resolution of N bits may represent 2^N distinct levels. Resolution is frequently given in bits. For instance, a 16-bit ADC may represent 2^16 levels, or 65,536, but an 8-bit ADC can represent 2^8 levels, or 256 distinct levels.

Accuracy

An important ADC characteristic called accuracy measures how closely the digital output of the ADC matches the actual analog input value. In terms of Least Significant Bits (LSBs), percentage of full scale, or absolute voltage levels, it represents the systematic inaccuracy or departure of the measured value from the real value. In applications requiring precise measurements, such instrumentation and sensor data gathering, high accuracy is essential.

Dynamic Range

Dynamic range, which defines the range of amplitudes that the ADC can properly convert from analog inputs to a digital representation, is a crucial characteristic for ADCs. The ADC's capacity to record both low-level and high-level signals without distortion or saturation is measured by dynamic range.

Monotonicity

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications.

Conversion Time:

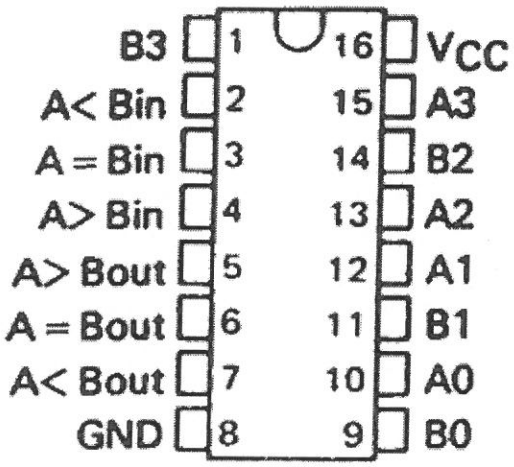
It is the time taken for the D/A converter to produce the analog output for the given binary input signal.

Settling time

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input.

8(a) Demonstrate the logic symbol and function table of comparator IC 7485

Pin Configuration and Logic Symbol of IC 7485



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A2 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

8(b) Explain the operation of the BCD-to-7- segment code converter with function table.

The result of a processing unit needs to be conveniently displayed to a user for its proper interpretation. The seven-segment LED display is a very common output device used to display decimal numbers. The seven segments of the display are labeled as a to g as shown in Figure 1(a). Displays representing decimal numbers from 0 to 9 are depicted in Figure 1(b). For example, segments a, b, d, e, and g should be lit up to display decimal .

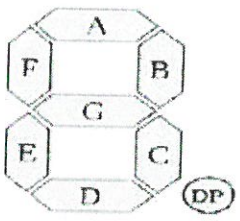


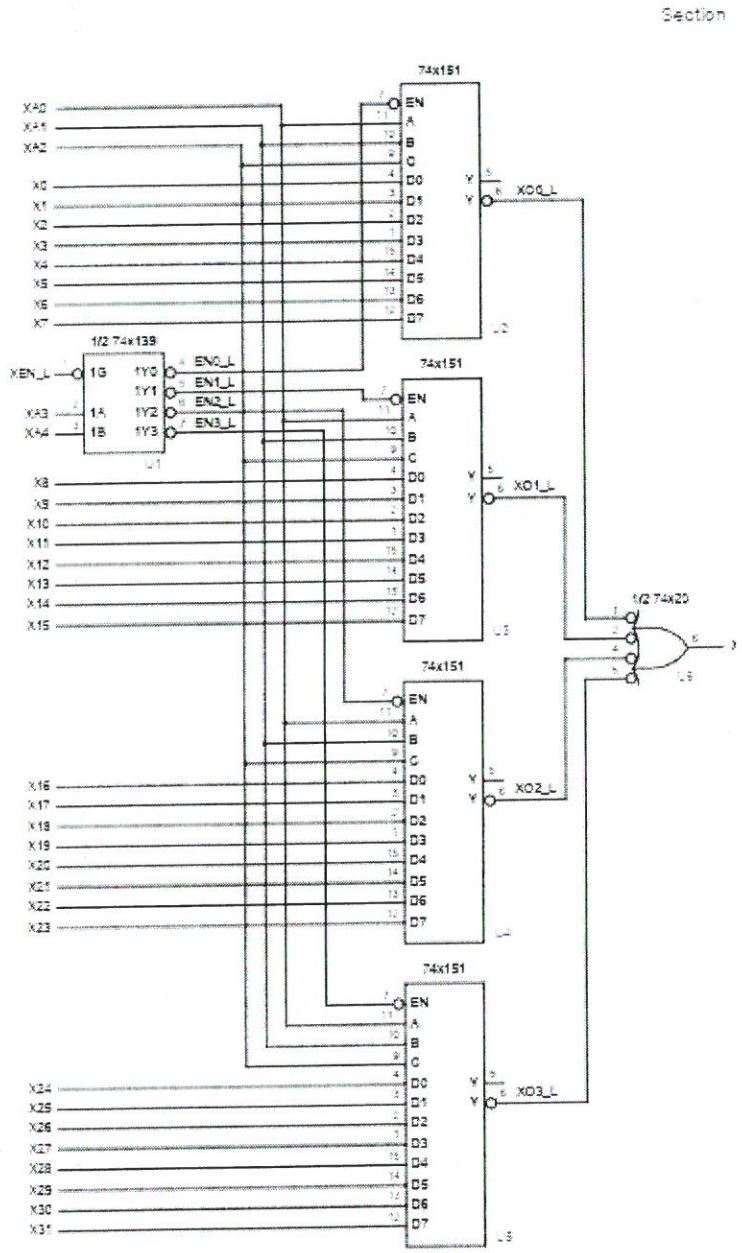
Figure a

Function Table

Suppose the binary input **ABCD** to the decoder and output a, b, c, d, e, f, & g for the display.

	INPUT				OUTPUT						
Digits	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

9(a) Realize 32:1 Multiplexer using 74151 ICs



9(b) Design a circuit to perform 8-bit binary addition using two 4 bit adder IC 7483s connected in cascade

IC 7483 is 4-bit binary full adder which accepts two 4-bit binary words $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ and a carry input (C_0) as inputs and produces a 4-bit binary sum output $S_3S_2S_1S_0$ and a carry output C_4.

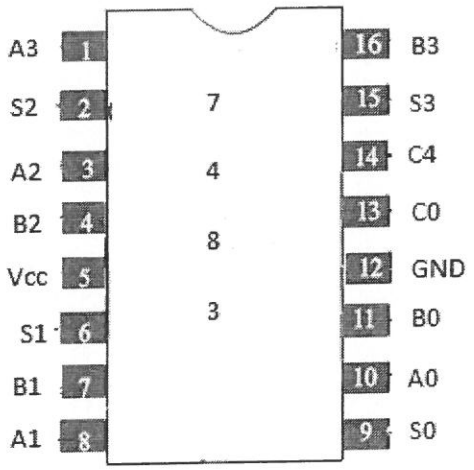


Figure 1

Cascading of two 7483 chips to achieve addition of two 8-bit numbers A = $A_8A_7A_6A_5A_4A_3A_2A_1$ and B = $B_8B_7B_6B_5B_4B_3B_2B_1$ to produce Sum = $S_8S_7S_6S_5S_4S_3S_2S_1$ and carry output C_9 .

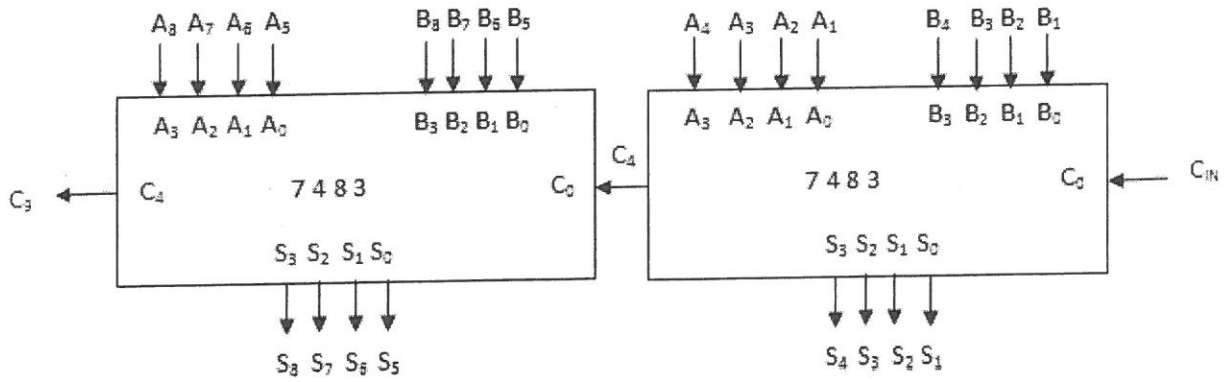


Figure 2

10(a) Discuss in detail about the differences between a latches and a flip-flops.

Difference Between Flip-Flop and Latch

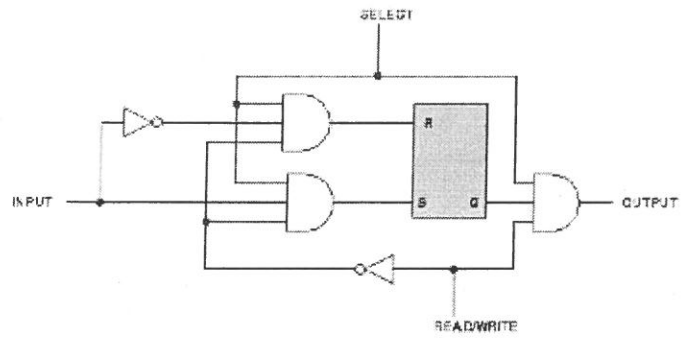
Flip-Flop	Latch
Flip-flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	Latch is also a bistable device whose states are also represented as 0 and 1.
It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.	It checks the inputs continuously and responds to the changes in inputs immediately.
It is a edge triggered device.	It is a level triggered device.
Gates like NOR, NOT, AND, NAND are building blocks of flip flops.	These are also made up of gates.
It forms the building blocks of many sequential circuits like counters.	These can be used for the designing of sequential circuits but are not generally preferred.
Flip-flop always have a clock signal	Latches doesn't have a clock signal
ex:D Flip-flop, JK Flip-flop	ex:SR Latch, D Latch

10(b) Explain the architecture of Random Access Memory (RAM). Highlight the differences between Static RAM and Dynamic RAM

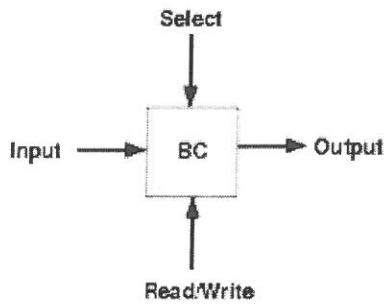
SRAM Design:

Design of a SRAM cell :

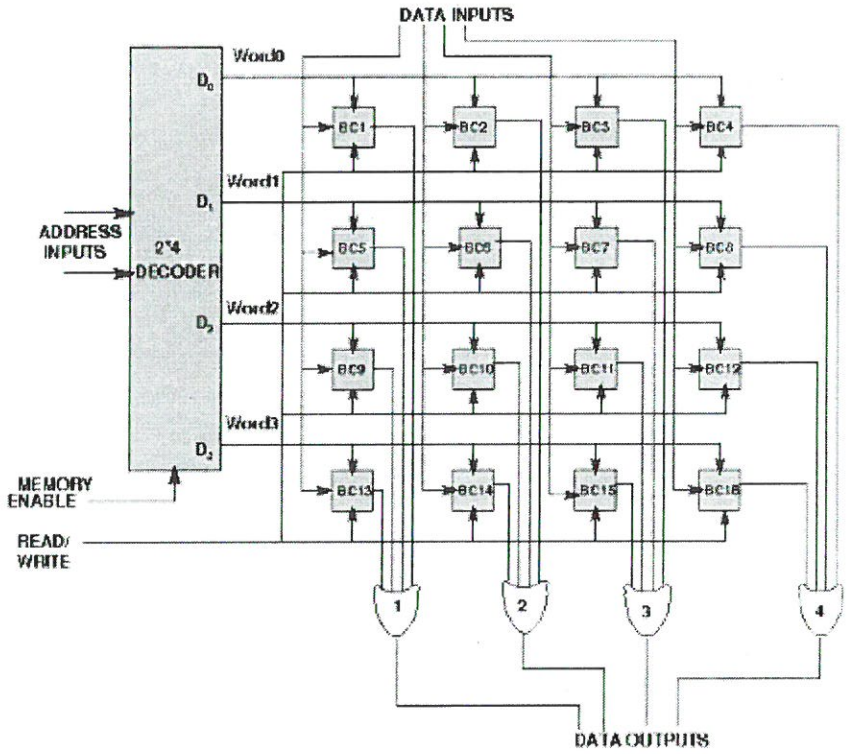
The binary cell has three inputs and one output. The select input enables the cell for reading or writing and the reda/write input determines the cell operation when it is selected. A 1 in the read/write input provides the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input provides the write operation by forming a path from the input terminal to the flip-flop. the logic diagram is-



Design of a 4X4 SRAM :



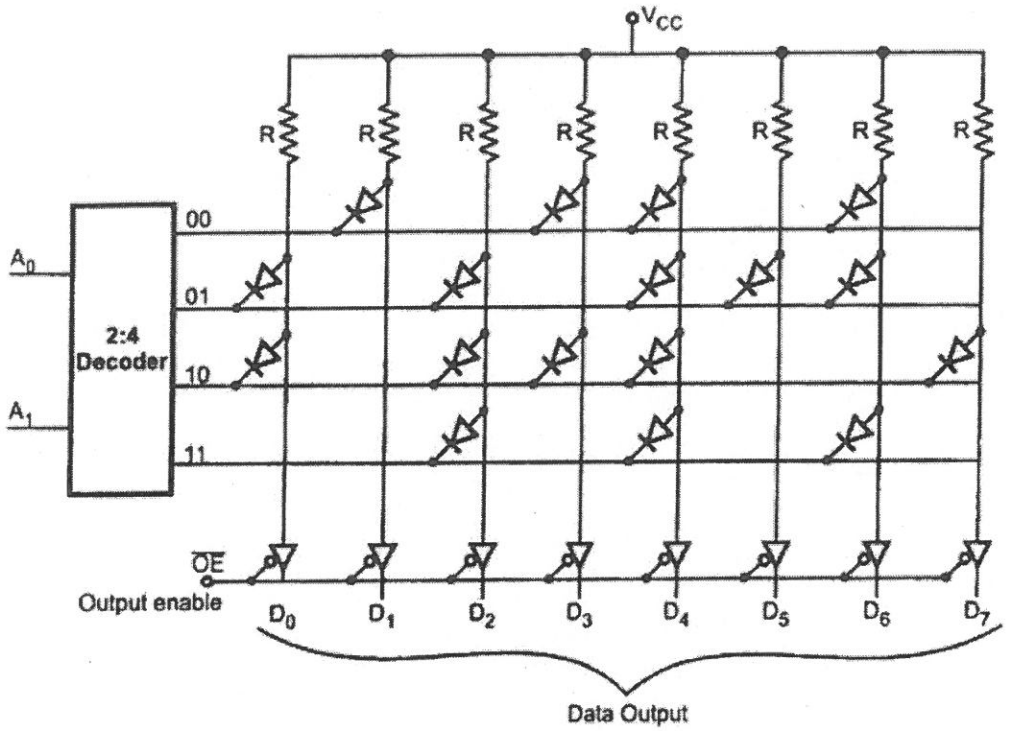
A memory with 4 words needs two address lines. The two address inputs go through a 2to4 decoder to select one of the four words. The decoder is enabled with the memory enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory enable at 1, one of the four words is selected, dictated by the value in the two address lines. Once a word has been selected, the read/write input determines the operation. the logic diagram is-



key difference between SRAM and DRAM:

Transistors are used to store information in SRAM. Capacitors are used to store data in DRAM. So in DRAM to store information for a longer time, the contents of the capacitor need to be refreshed periodically.

11(a) Discuss the Principle of operation of ROM.



Diode ROM Memory consists of only diodes and a decoder. As shown in the Fig. address lines A0 and A1 are decoded by 2 : 4 decoder and used to select one of the four rows. As decoder output is active low, it places a logic 0 on the selected row. Each output data line goes to logic 0 if a diode connects the output data column to the selected row. Data is available on the output data lines only when output enable (OE) signal is low.

11(b) Design and explain the working of a decade counter using IC 7490. Draw its internal block diagram and truth table.

Asynchronous Decade Counters

A common modulus for counters with truncated sequences is ten. A counter with ten states in its sequence is called a decade counter. Once the counter counts to ten (1010), all the flip-flops are being cleared. Notice that only Q1 and Q3 are used to decode the count of ten. This is called

partial decoding, as none of the other states (zero to nine) have both Q1 and Q3 HIGH at the same time.

Asynchronous counter circuit design is based on the fact that each bit toggle happens at the same time that the preceding bit toggles from a "high" to a "low" (from 1 to 0).

Decade Counter Truth Table

Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

IC7490 Decade Counter