PVP 23

Code: 23EC4501A

III B.Tech - I Semester - Regular Examinations - NOVEMBER 2025

DIGITAL SYSTEM DESIGN THROUGH HDL
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

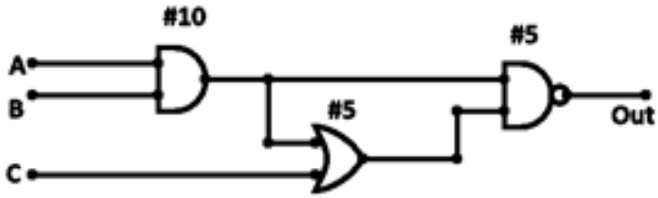
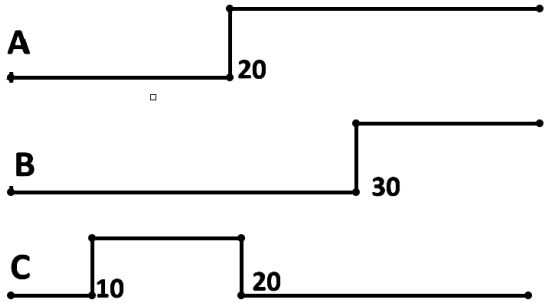
PART – A

		BL	CO
1.a)	Discuss the mean by Z in Verilog HDL, explain with a case study.	L2	CO1
1.b)	Describe the difference between the operators "&&" and "&".	L2	CO1
1.c)	Analyze the output of y1 and y2, if a = 110X and b = 110X assign y1 = (a ==b); assign y2 = (a===b);	L4	CO2
1.d)	Perform the binary addition of +6 and -3 and verify your answer.	L2	CO2
1.e)	What is lowest level of abstraction in Verilog HDL?	L2	CO3
1.f)	Predict the truth tables of OR gate including 0, 1, X and Z.	L2	CO3
1.g)	Identify the operators required to design a one-bit comparator.	L2	CO4
1.h)	Differentiate between blocking and non-blocking statements.	L2	CO4

1.i)	Is it possible to include both level-sensitive and edge-sensitive signals in the sensitivity list of a single always block.	L4	CO5
1.j)	Explain the Testing.	L2	CO5

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	Discuss the different complier directives in Verilog HDL.	L2	CO1	5 M
	b)	Explain Module structure in Verilog HDL.	L2	CO1	5 M
		OR			
3	a)	Describe the different Data types in Verilog HDL.	L2	CO1	5 M
	b)	Implement XOR gate using basic gate primitives.	L2	CO1	5 M
		UNIT-II			
4	a)	Explain the differences between sequential and parallel blocks with a case study.	L2	CO2	5 M
	b)	Write a Verilog HDL code to implement 4 bit Register.	L2	CO2, CO3	5 M
		OR			
5	a)	Develop a Verilog code to implement the D flip flop. Name the module as D_FF.	L4	CO2	5 M
	b)	Design Verilog HDL program 4 bit binary counter using behavioural modelling.	L4	CO2, CO3	5 M
		UNIT-III			
6		Implement a mux_2to1 circuit using a conditional operator and then use the module instantiation to implement mux_4to1 using mux_2to1.	L4	CO2, CO3	10 M

	OR			
7	Develop the Data flow Verilog model to design the circuit with delay constraints. Write stimulus block to excite the inputs shown below. Also draw the output waveform.  circuit  Input excitation (timescale is ns)	L4	CO2, CO3	10 M
	UNIT-IV			
8	In the traditional Korean game *Ddakji*, a player wins if they successfully flip the opponent's tile **three times in a row**. Each successful flip is represented by a binary 1, and each failed flip is represented by a binary 0. Design a Mealy/Moore **sequence detector** using **Verilog HDL** that detects three consecutive successful flips in a serial input stream. Design Requirements: i. The design should use a **Finite State Machine (FSM)**. ii. The detector should not allow **overlapping sequences**.	L4	CO4	10 M

	iii. Use the following input/output signals: ○ clk – Clock input ○ rst – Asynchronous active-high reset ○ flip – 1-bit input (success = 1,fail = 0) win – 1-bit output, high only when the player wins.				
	OR				
9	Design the Verilog HDL for User Defined Primitive with example.		L4	CO4	10 M
	UNIT-V				
10	a)	Analyze the test bench to verify the functionality of 3 to 8 decoder with an enable pin.	L4	CO5	5 M
	b)	Explain DUT with block diagram.	L4	CO5	5 M
	OR				
11	a)	Design the test bench to verify the functionality of D Flip-flop with a reset pin.	L4	CO5	5 M
	b)	Explain the difference between output Q; and output reg Q;	L4	CO5	5 M