| UNIT-V | | | | | |
|---|---|---|---|---|---|
| 10 | a) | Explain the basic operation of a 565 PLL using its functional block diagram. | L3 | CO3 | 5 M |
| | b) | Draw the block diagram of a PLL and explain the function of Phase detector, low-pass filter and VCO. | L3 | CO3 | 5 M |
| OR | | | | | |
| 11 | a) | Explain the operation of a Successive approximation ADC. | L4 | CO4 | 5 M |
| | b) | Illustrate the following ADC and DAC specification: resolution, Linearity, accuracy, monotonicity, settling time. | L4 | CO4 | 5 M |



PVP 23

Code: 23ES1401

**II B.Tech - II Semester – Regular Examinations - MAY 2025**

# ANALOG CIRCUITS
## (ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours    Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level    CO – Course Outcome

## PART – A

| | | BL | CO |
|---|---|---|---|
| 1.a) | Build a circuit of a series positive clipper. | L2 | CO1 |
| 1.b) | Sketch a collector to base bias circuit. | L2 | CO1 |
| 1.c) | Define the h-parameters hi, ho, $h_f$, and $h_r$ | L1 | CO1 |
| 1.d) | Illustrate the approximate formulas for $A_i$, $R_i$, $A_v$, $R_o$ | L2 | CO1 |
| 1.e) | List the ideal values of CMRR, Input offset current, Input offset voltage. | L1 | CO1 |
| 1.f) | Write the applications of oscillator. | L1 | CO1 |
| 1.g) | Give the output voltage formula for an integrator and differentiator. | L2 | CO1 |
| 1.h) | List the applications of OP-AMP. | L1 | CO1 |
| 1.i) | Define the phase locked loop. | L1 | CO1 |
| 1.j) | Classify the different types of DAC. | L1 | CO1 |

## PART – B

| | | | BL | CO | Max. Marks |
|---|---|---|---|---|---|
| | | **UNIT-I** | | | |
| 2 | a) | Explain the operation of a diode clipper in a series circuit for positive clipping. | L2 | CO1 | 5 M |
| | b) | Describe a diode clipping circuit that clips an input signal at two independent levels with its transfer characteristics. | L3 | CO2 | 5 M |
| | | **OR** | | | |
| 3 | a) | Illustrate the collector to base bias technique for a BJT with necessary circuit diagram. | L3 | CO2 | 5 M |
| | b) | Consider the self bias circuit where $V_{cc}$=23V, $R_C$=12KΩ, $R_1$ = 90KΩ, $R_2$ = 10KΩ $h_{fe}$=55, $V_{BE}$=0.6V. Determine (i) Operating point (ii) Stability Factor. | L3 | CO2 | 5 M |
| | | **UNIT-II** | | | |
| 4 | a) | Derive the expressions for $Z_i$, $A_v$, $A_I$ and $Y_o$ for a Common-Emitter Configuration. | L3 | CO2 | 5 M |
| | b) | Relate the approximate conversion formulas for CB, CE, CC configurations and represent with its two port network. | L3 | CO2 | 5 M |
| | | **OR** | | | |
| 5 | | A CE amplifier has the h parameter given by $h_{ie}$=1KΩ, $h_{re}$=2x$10^{-4}$, $h_{fe}$=50 and $h_{oe}$=25μmhos. If both the load and source of internal resistance 1KΩ. Determine i) Current gain ii)Voltage gain | L4 | CO4 | 10 M |



| | | | | | |
|---|---|---|---|---|---|
| | | **UNIT-III** | | | |
| 6 | a) | Explain the operation of a crystal oscillator and write the expression for its frequency of oscillation. | L2 | CO3 | 5 M |
| | b) | Calculate the frequency of oscillation for a Wien bridge oscillator with R=6KΩ and C=46nF | L3 | CO3 | 5 M |
| | | **OR** | | | |
| 7 | a) | Develop an adder circuit and obtain the output voltage of an adder circuit using 741 OP-AMP | L4 | CO4 | 5 M |
| | b) | Analyze the circuit of a V to I and I to V convertor and obtain its output expression. | L4 | CO4 | 5 M |
| | | **UNIT-IV** | | | |
| 8 | a) | Describe the basic operation of an a integrator using 741 OP-AMP | L2 | CO3 | 5 M |
| | b) | Explain the working of a sample and hold circuit with waveform. | L2 | CO3 | 5 M |
| | | **OR** | | | |
| 9 | a) | Describe the working of a non-inverting comparator with waveforms. | L3 | CO3 | 5 M |
| | b) | Draw the circuit of a triangular wave generator using a 741 OP-AMP and explain its operation. | L2 | CO3 | 5 M |

II B.Tech II-Sem Regular exam, May 2025
Subject: Analog Circuits (20ES1401)
Dept: EEE, Regulation: PVP 23

Scheme of Valuation – PART: B

2.a. Circuit Diagram – 2M
operation & condition – 1M
waveforms – 2M

2.b. Circuit diagram – 2M
Operation & conditions – 1M
Waveforms – 2M

3.a. Circuit Diagram – 3M
Operation – 1M
Stability factor – 1M

3.b. Calculation of $V_T$ and $R_T$ or $R_B$ – 3M
$I_C$ value – 1M
$S$ value – 1M

4.a. Circuit diagrams – 2M
$A_I$, $Z_i$, $A_V$, $Y_o$ derivation – 3M

4.b. Circuit diagrams – 2M
Conversion formulas – 3M

5. $A_I$ value formula & calculation – 5M

$A_V$ value formula & Calculation – 5M

6.a. Crystal oscillator diagrams – 3M
operation – 1M
graph – 1M

6.b. given data – 1M
$f_o$ formula – 2M
Calculation & answer – 2M

7.a. Circuit diagram — 3M

Analysis & $V_0$ — 2M

7.b. V–I converter circuit diagram — 2M

operation — 1M

I–V converter circuit & operation — 2M

8.a. Basic Circuit diagram — 2M
integrator

operation — 1M

graph — 2M

8.b. Circuit Diagram — 2M

operation — 1M

waveforms — 2M

9.a. Circuit diagram — 2M

Conditions — 1M

waveforms — 2M

9.b. Circuit diagram & waveforms — 3M

operation & formulas — 2M

10.a. 565 IC pin diagram & operation — 3M)

Block diagram — 2M

10.b. PLL Block diagram — 3M

operation — 2M

11.a. Circuit Diagram — 3M

Explanation — 2M

11.b. Resolution — 2M

Linearity — 1M

Accuracy — 1M

monotonicity — 1M

II B·Tech II – Sem Regular Exam, May 2025

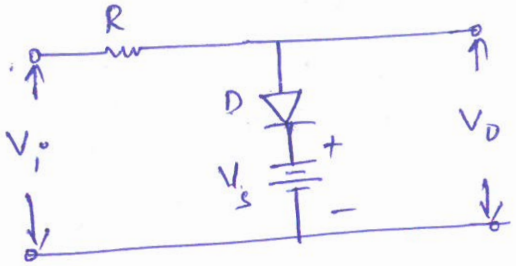
Subject: Analog Circuits (20ES1401)

Dept: EEE , Regulation: PVP23

$\boxed{\text{Key}}$

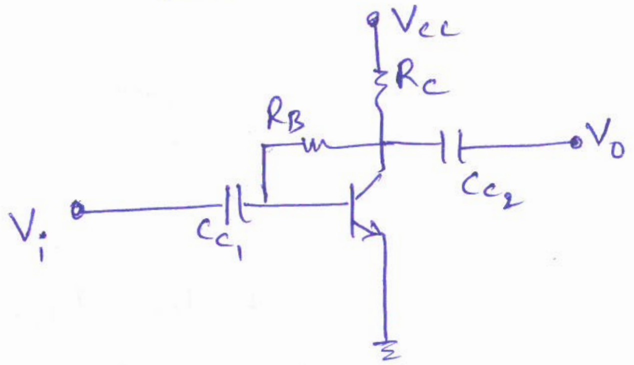
## Part – A

1. a)




(2m)

b)




(2m)

c) $h_i = \frac{v_1}{i_1}\Big|_{v_2=0}$ ; $h_r = \frac{v_1}{v_2}\Big|_{i_1=0}$ ; $h_f = \frac{i_2}{i_r}\Big|_{v_2=0}$ , $h_o = \frac{i_2}{v_2}\Big|_{i_1=0}$ (2m)

d) $A_I = \frac{-h_f}{1+h_o R_L}$ , $R_i \simeq h_i$ (2m)

$A_V = A_I \frac{R_L}{R_i} = -\frac{h_f R_L}{h_i}$ ; $R_o = \infty$

e) CMRR = $\infty$

input offset current = 0 A (2m)

" " Voltage = 0 A

f) in communication systems, signal generators, Audio systems (2m)

g) $V_o \propto \frac{dv_i}{dt} \Rightarrow V_o = -R_f C_1 \frac{dV_i}{dt}$ for differentiator (1m)

$V_o \propto \int v_i \Rightarrow V_o = -\frac{1}{R_1 C_f}\int v_i\, dt$ for integrator (1m)

(h) op-Amp's used in voltage amplifier, current amplifier, instrumentation amplifiers, adders, subtractors, differentiators, V to I and I to V converters, comparators, wave form generators.

(2m)

(i) an electronic circuit used for electronic frequency control by comparing phase of input signal with the phase of a feedback signal to match input phase and frequency.

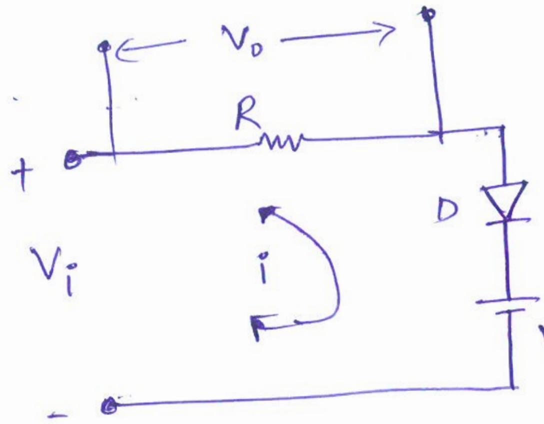
(2m)

(j) R-2R ladder
Inverted R-2R ladder
weighted resistor

(2m)

## part-B

2(a)




Series circuit for clipping of a portion of the positive cycle

(2m)

the use of KVL in the circuit results in a diode voltage $V = -(V_i + V_s)$.

Since $V > V_\gamma$ determine the ON state of a diode when $V_i < -(V_s + V_\gamma)$

Current flowing through R in ON state of a diode

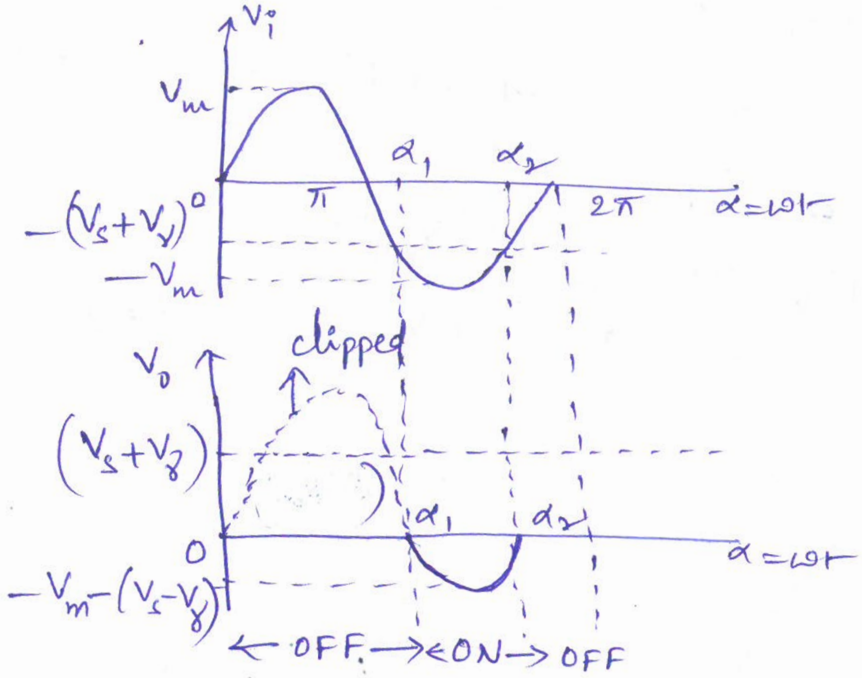
$$i = \frac{V_i + V_s + V_\gamma}{R + R_f} \simeq -\frac{(V_i + V_s + V_\gamma)}{R} \quad \text{if } R >> R_f.$$

Since $i = 0$ in OFF state of the diode and $V_o = -iR$

the output voltage of a circuit for the entire can be given as

$$V_0 = \begin{cases} v_i + (V_s + V_\gamma) & \text{for } v_i < -(V_s + V_\gamma) \\ 0 & \text{for } v_i > -(V_s + V_\gamma) \end{cases} \quad (1m)$$

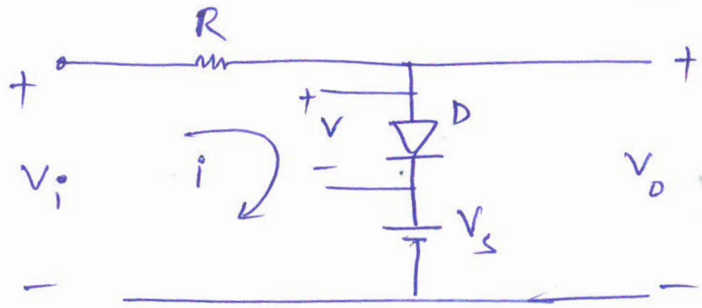
where the input and output voltages are measured with respect their negative terminals as shown in the circuit and corresponding wave forms are shown




(2m)

(or)

parallel circuit for clipping of a portion of the ~~portion of~~ positive amplitude of input signal




the voltage across the diode for $i=0$ is $v = v_i - V_s$.

Since $v > V_\gamma$ corresponds to ON state of the diode, this condition can be defined in terms of the input signal votage as

$$v_i > V_s + V_\gamma$$

The diode will be in OFF state for $v_i < V_s + V_\gamma$. The current flows through diode in ON state can be obtained by KVL

$$i = \frac{v_i - (V_s + V_\gamma)}{R + R_f}$$

So $V_o$ during ON state of the diode is

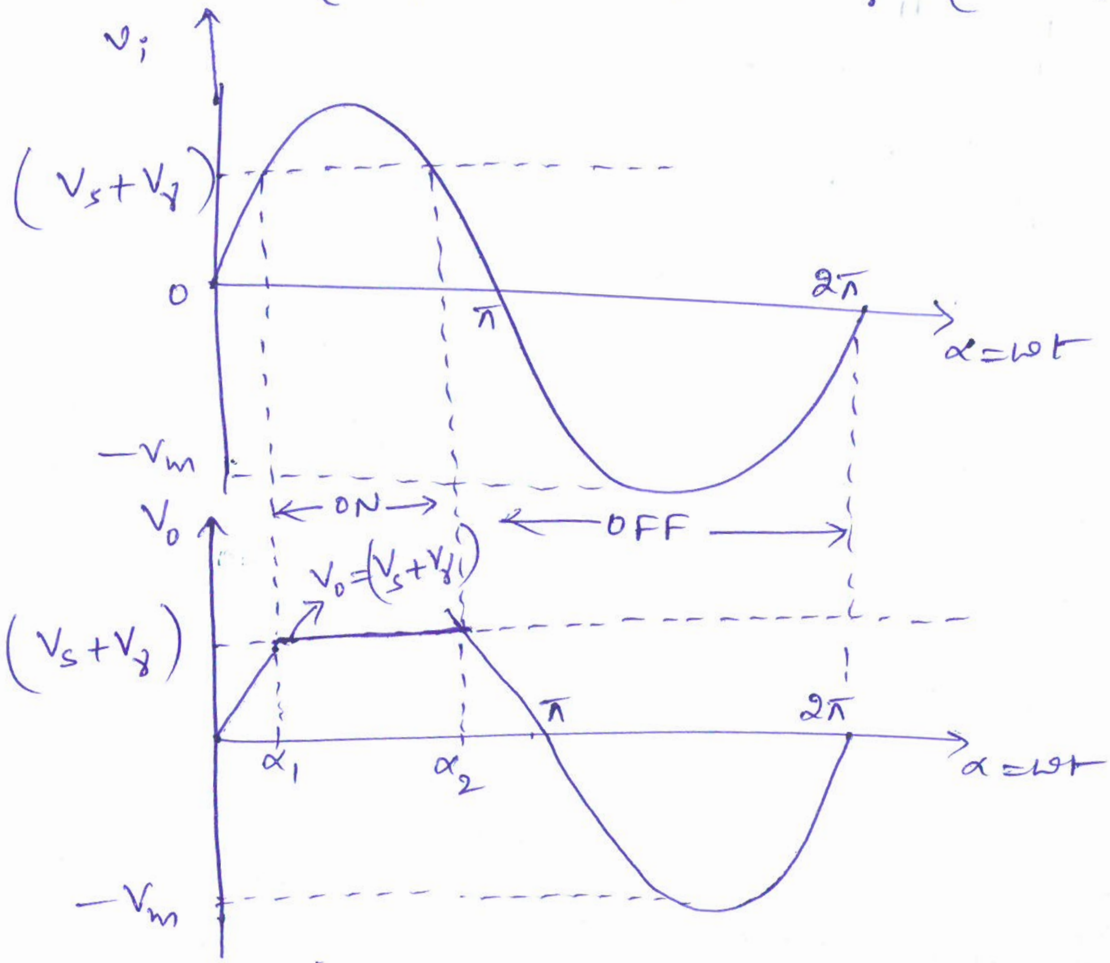
$$v_o = (V_s + V_\gamma) + iR_f$$

$$= (V_s + V_\gamma) + [v_i - (V_s + V_\gamma)] \frac{R_f}{R + R_f}$$

$$v_o \simeq (V_s + V_\gamma) \text{ if } R >> R_f \text{ in a circuit}$$

$v_o = v_i$ when the diode is in OFF state. Thus the output during entire part of input is

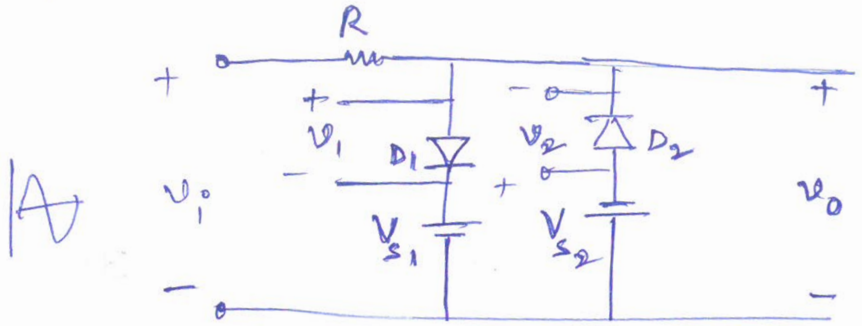
$$v_o = \begin{cases} V_s + V_\gamma & \text{for } v_i > V_s + V_\gamma \text{ (Diode ON)} \\ v_i & \text{for } v_i < V_s + V_\gamma \text{ ( " OFF)} \end{cases}$$




Note: please consider either series (or) parallel positive clipper as positive parallel clipper is given in micro syllabus so may be award marks.

... independent levels, Consider parallel c...
with diodes used to remove an arbitrary portion of +ve cycles and -ve
Cycles of an input ac signal

(2m)




$v_1$ and $v_2$ are voltag...
across $D_1$ and $D_2$ ...
assume no current ...
through circuit ...

$v_i > V_{s_1} + V_{\gamma_1}$ ; $D_1$ ON
$v_i < V_{s_1} + V_{\gamma_1}$ ; $D_1$ OFF

and

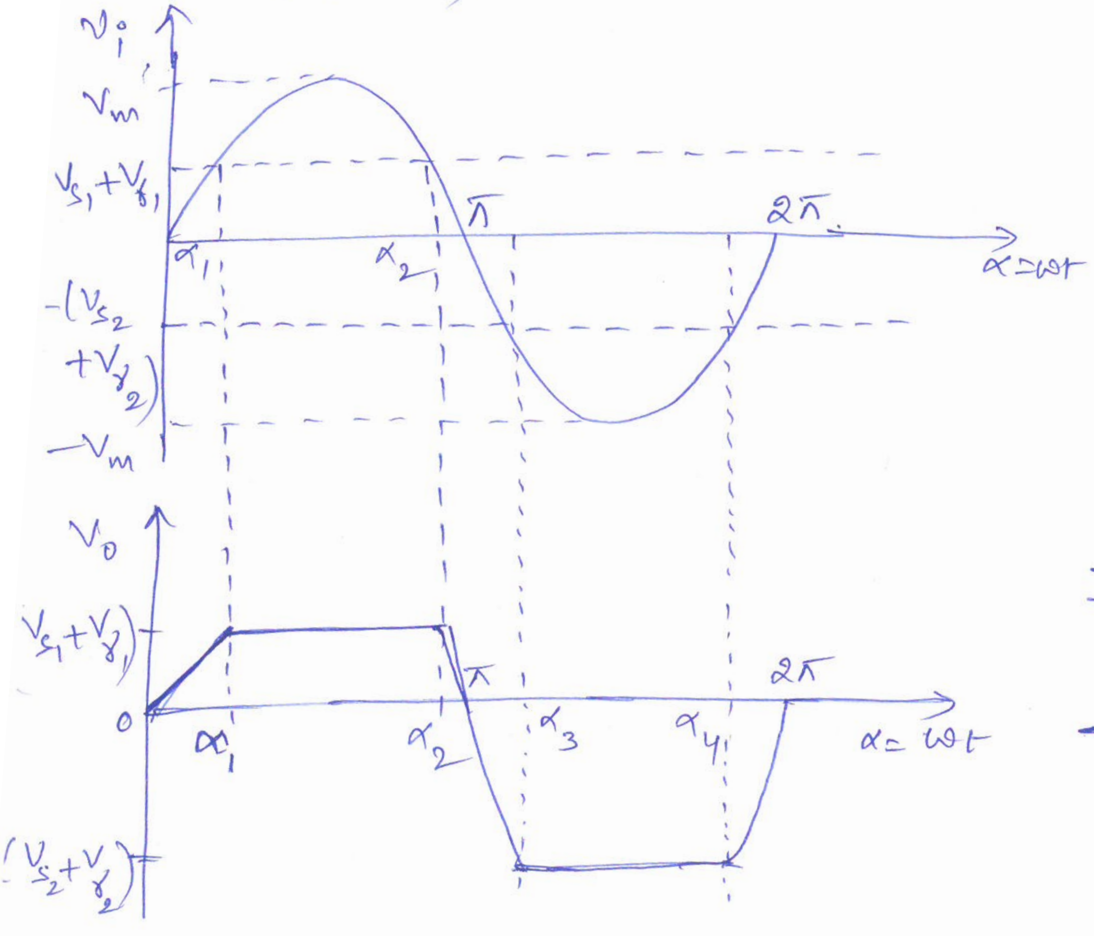
$v_i < -(V_{s_2} + V_{\gamma_2})$ ; $D_2$ ON
$v_i > -(V_{s_2} + V_{\gamma_2})$ ; $D_2$ OFF

where $V_{\gamma_1}$ and $V_{\gamma_2}$ are cut in voltages of $D_1$ and $D_2$

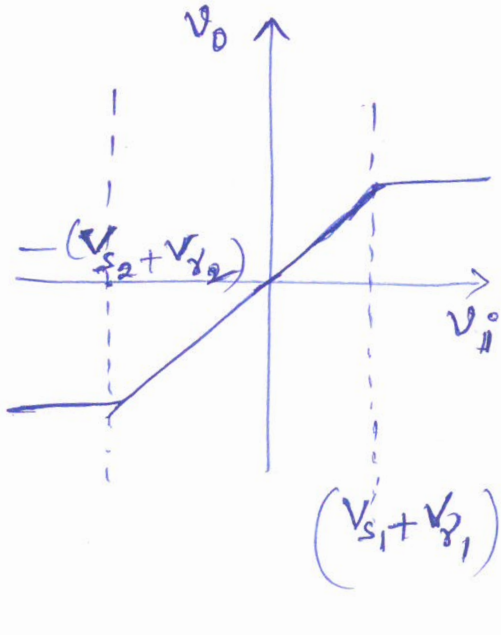
(1m)

| Input | Conducting states of $D_1$ and $D_2$ | output |
|---|---|---|
| $v_i < -(V_{s_2} + V_{\gamma_2})$ | $D_1$ OFF and $D_2$ ON | $V_0 = -(V_{s_2} + \ldots$ |
| $-(V_{s_2} + V_{\gamma_2}) < v_i < (V_{s_1} + V_{\gamma_1})$ | $D_1$ OFF, $D_2$ OFF | $V_0 = v_i$ |
| $v_i > (V_{s_1} + V_{\gamma_1})$ | $D_1$ ON & $D_2$ OFF | $V_0 = V_{s_1} + V_{\ldots}$ |

(2m)



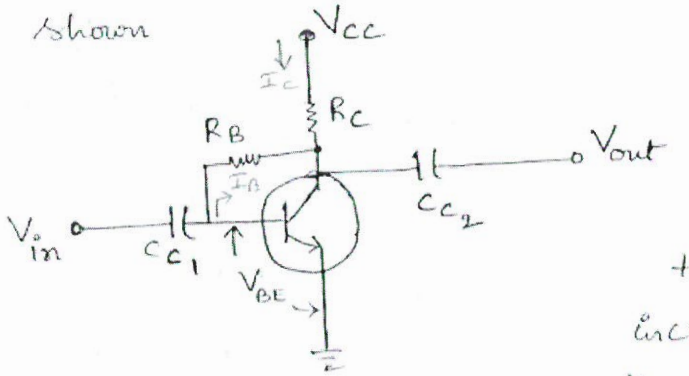

Transfer character...
of two level clipper



3.a

Collector to Base Bias (or) Collector FeedBack Bias

A CE amplifier using collector to Base bias circuit is shown




If $I_C$ increases due to either increase of temperature (or) higher $\beta$ value then the voltage drop across $R_C$ increases, thereby reducing the $V_{CE}$ (3 m)

Therefore $I_B$ decreases which compensate the increase in $I_C$. Thus greater stability is obtained

the loop equation for this circuit is (1m)

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

$$\Rightarrow \frac{dI_B}{dI_C} = \left(\frac{-R_C}{R_C + R_B}\right)$$

$$\text{Stability factor } (S) = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)} \qquad \left(\because S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}}\right)$$

(1 m)

If S value is small then more stability.

So Stability can be improved by making $R_B$ small (or) $R_C$ large.

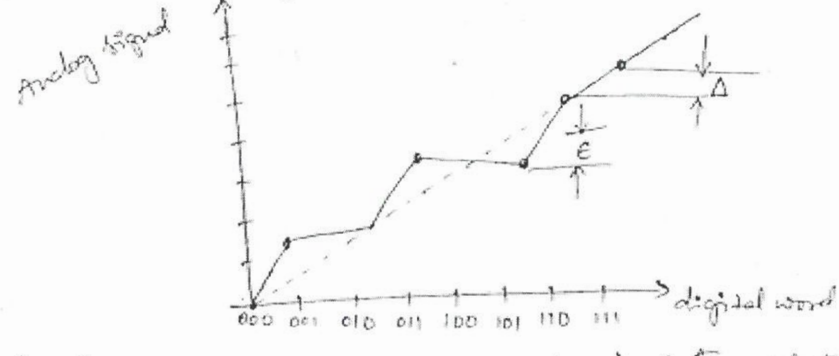
If $R_C$ is very small then $S = (1+\beta)$

then stability is very poor.

Hence the value of $R_C$ must be quite large for good stabilization.

ii) Linearity :- It is an measurement of accuracy and tells how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in digital input should produce equal increment in ~~digital~~ output and the transfer curve should be linear. However, in practical DAC, output voltages do not fall on a straight line because of gain and offset errors as shown

(1 M)

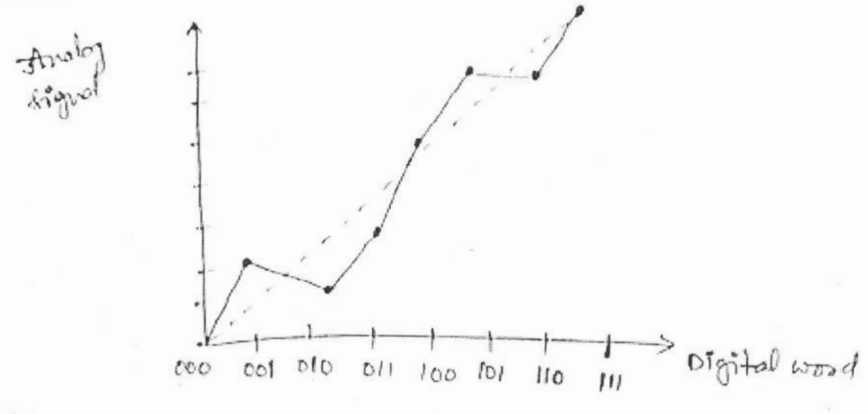



The linearity errors measures the deviation of the actual output from the fitted line and is given by ε/Δ as shown in graph.

iii) Accuracy :- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. The accuracy of a converter is also specified in terms of LSB increments (or) % of full scale voltage. (1 M)

iv) Monotonicity :- whose analog output increases for an increase in digital input. The transfer curve for non-monotonic DAC is shown as

(1M)




Since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications otherwise oscillations can produce.

At the start of a conversion cycle, the SAR is reset by holding the Start (S) signal high. On the first cycle, pulse LOW to HIGH transition, the MSB $Q_7$ of the SAR is set. The D/A converter then generates an analog equivalent to $Q_7$, which is compared with the analog input $V_{in}$. If the comparator output is low, the DAC output $> V_{in}$ and the SAR will clear its MSB $Q_7$. On the other hand, if comparator output is high, the D/A output $< V_{in}$ and the SAR will keep MSB $Q_7$ set.

In any case, on the next clock pulse LOW to HIGH transition, the SAR will then either keep or reset the bit $Q_6$. This process is continued until the SAR tries all the bits. As soon as LSB $Q_0$ is tried, the SAR forces the conversion complete (CC) signal HIGH to indicate that the parallel output lines contain valid data.

**11.b.**

## DAC/ADC Specifications

**i) Resolution:** It is the smallest change in voltage which may be produced at the output (or input) of a converter. For example, an 8-bit D/A converter has $2^8 - 1 = 255$ equal intervals. Hence the smallest change in output voltage is $\frac{1}{255}$ of the full scale output range. In short, the resolution is the value of LSB.

(2M)

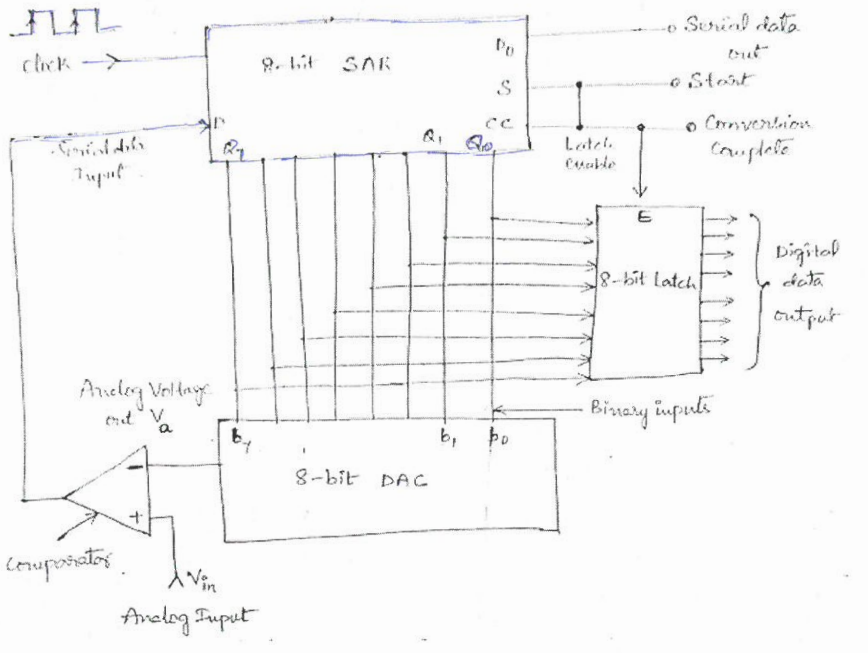
$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment}$$

An 8-bit DAC is said to have
→ 8-bit resolution
→ a resolution of 0.392% of full scale
→ a resolution of 1 part in 255.

* Similarly the resolution of an ADC is defined as the smallest change in analog input for a one bit change at the output.

The signal $V_c$ shifts VCO frequency in a direction to reduce the frequency difference between $f_s$ and $f_o$. Once this action starts, we say that the signal is in capture range. The VCO continues to change frequency till its output frequency is exactly the same as input signal $f_s$. The circuit then said to be locked. Once locked, the o/p frequency $f_o$ of VCO is identical to $f_s$ except for a finite phase difference $\phi$. This $\phi$ generates a corrective control voltage $V_c$ to shift VCO frequency from $f_o$ to $f_s$ and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through 3 stages (i) free running (ii) capture (iii) locked (or) Tracking.

**11.a.**



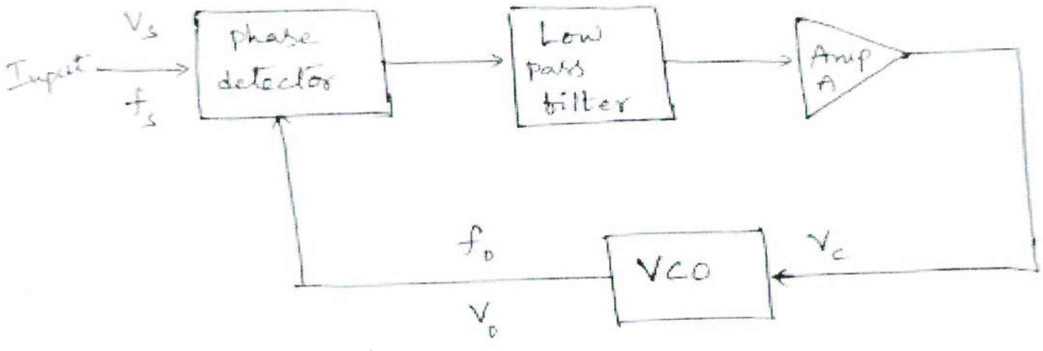

(3M)

The analog output $V_a$ of DAC is then compared to an analog input signal $V_{in}$ by the comparator. The output of a comparator is a serial data input to the SAR. The SAR then adjusts its digital output (8 bits) until it is equivalent to analog input $V_{in}$. The 8-bit latch at the end of conversion holds onto the resultant digital data output. The circuit works as follows. (2M)

**10.b.**

The basic schematic of PLL is shown

(3m)




PLL mainly contains

1. phase detector / comparator
2. A low pass filter
3. An error amplifier
4. A voltage controlled oscillator (VCO).

(2m)

VCO is a free running multivibrator and operates at a set frequency $f_0$ called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage $V_c$ to an appropriate terminal of IC.

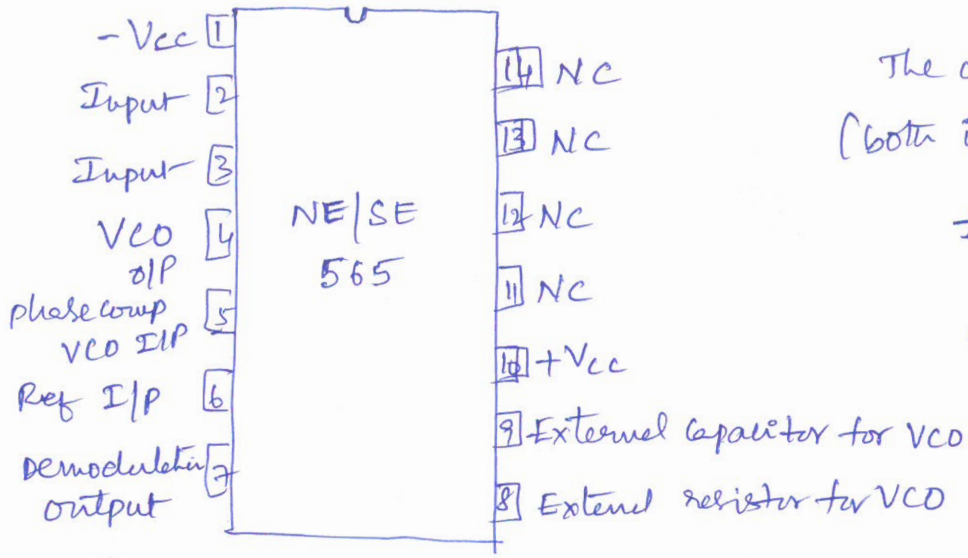
The frequency deviation is directly proportional to dc control voltage and hence it is called a voltage controlled oscillator (or) VCO.

If an input signal $V_s$ of frequency $f_s$ is applied to PLL, the phase detector compares the phase and frequency of incoming signal to that of output $V_0$ of VCO. If the two signals are different in phase / frequency then error voltage $V_e$ is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_0)$ and difference $(f_s - f_0)$ components at its output. The high frequency component $(f_s + f_0)$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage $V_c$ to VCO.

## (10.a) IC PLL 565

565 PLL is available in a 14-pin DIP package and in 10 pin metal can package. The pin configuration and block diagram are

(3M)




The output frequency of VCO (both inputs 2,3 is given by

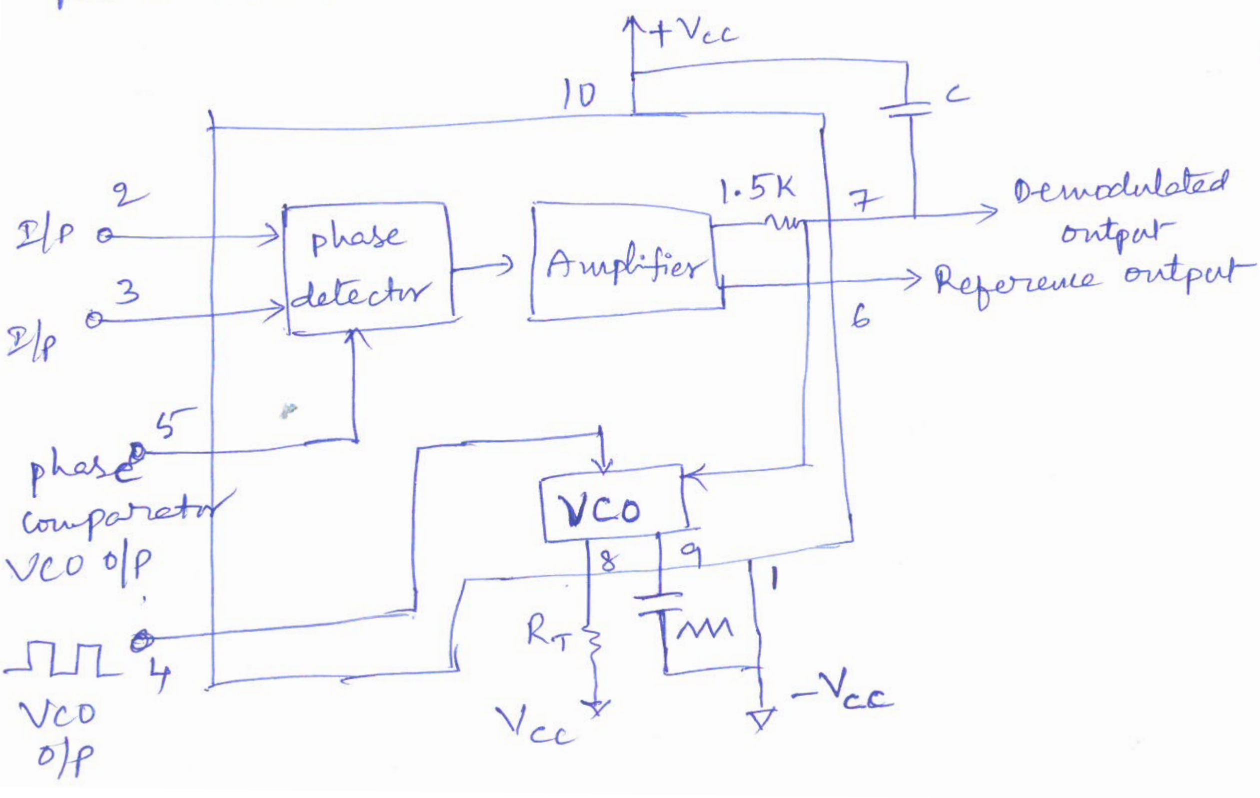
$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz}$$

where $R_T$ = external resistor connected to pin 8

$C_T$ = external capacitor connected to pin 9

A value between 2KΩ and 20KΩ is connected between 8 pins is recommended for $R_T$. The VCO free running frequency is adjusted with $R_T$ and $C_T$ to be at the centre of input frequency range. It may be seen that PLL is internally broken between VCO output and phase comparator input. A short circuit between pins 1 and 5 connects the VCO output to the phase comparator so as to compare $f_0$ with the input signal $f_i$. A capacitor C is connected between pin 7 and pin 10 to make LPF with internal resistance of 3.6KΩ

(2M)



9.b.

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. . Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor $C_2$ in the feedback circuit decreases at high frequencies. A resistance $R_4$ is connected across $C_2$ to avoid the saturation problem at low frequencies as in the case of practical integrator.

(3m)

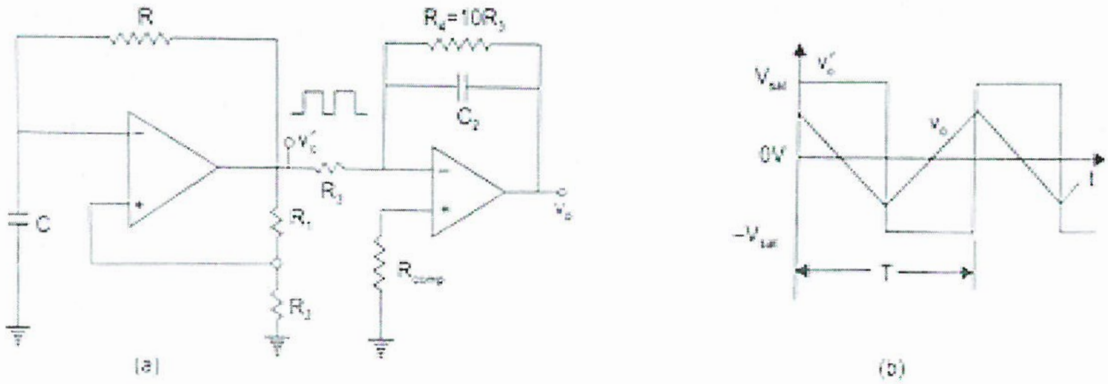



Fig. (a) Triangular waveform generator, (b) Output waveform

zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point $P$ during the time when output of $A_1$ is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right]$$

At $t = t_1$, the voltage at point $P$ becomes equal to zero. Therefore,

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat})$$

(2m)

Similarly, at $t = t_2$, when the output of $A_1$ switches from $-V_{sat}$ to $+V_{sat}$,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat})$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o\,(\mathrm{pp}) = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_3}V_{sat}$$

The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$. Putting the values in the basic integrator equation

$$T = 2R_1C_1\frac{v_o\,(\mathrm{pp})}{V_{sat}}$$

Putting the value of $v_o$ (pp) from Eq. (5.21), we get

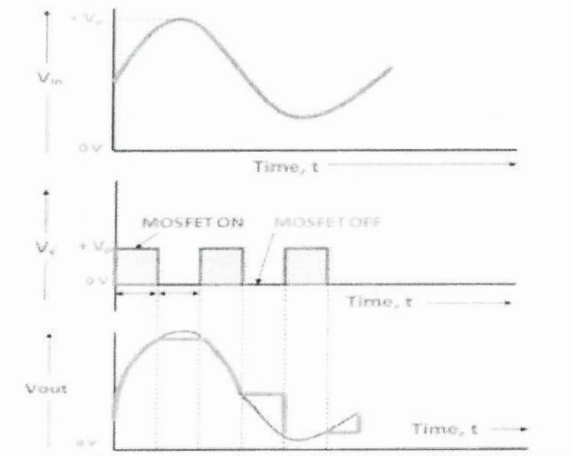
$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation $f_o$ is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$$

Therefore, the triangular wave oscillates between + 7V and – 7V.

Sample and Hold circuit efficiently captures and holds analog signals using the interplay between the MOSFET, capacitor, and operational amplifier. The MOSFET acts as a switch, the capacitor stores the charge, and the operational amplifier ensures the integrity of the held signal during the holding period, making it a crucial component in various electronic applications.



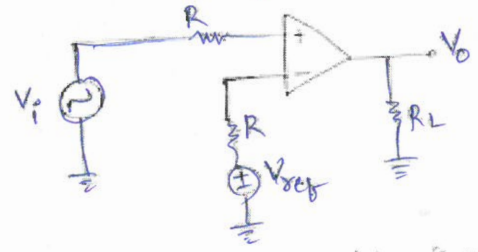
Input and Output Waveforms of Sample and Hold Circuit

(2m)

**9.a.**

a Non inverting Comparator Circuit

comparator circuit is shown



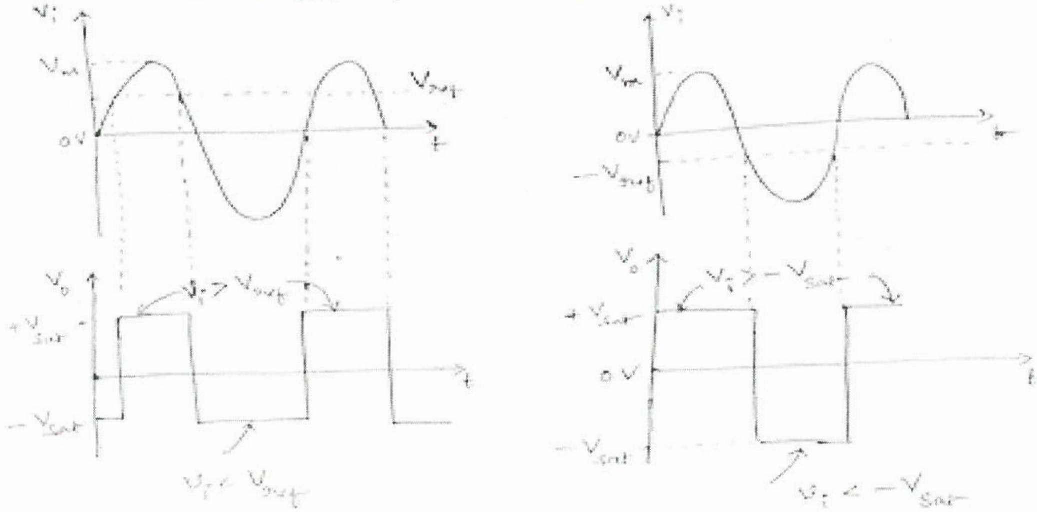

(2M)

A fixed reference voltage $V_{ref}$ is applied to (−) input and a time varying signal $v_i$ is applied to (+) input.

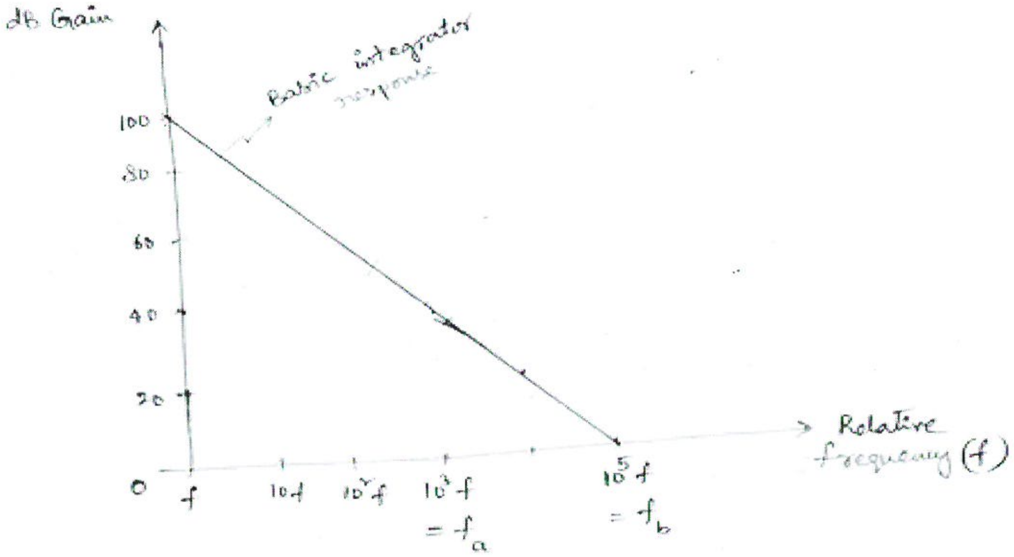
(1M)

$V_o = -V_{sat}$ if $v_i < V_{ref}$

$V_o = +V_{sat}$ if $v_i > V_{ref}$




(2M)




(2m)

In above graph, $f_b$ is the frequency at which the gain is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

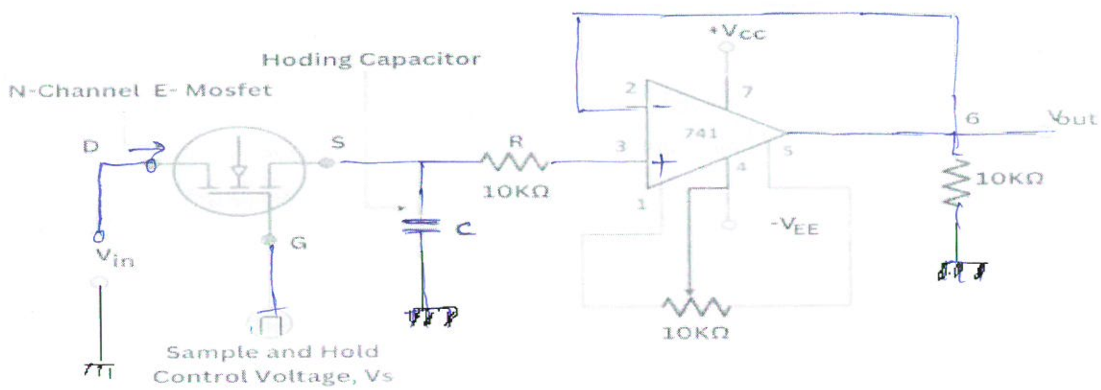
**8.b.**

Understanding how a sample and hold circuit works is like figuring out the roles of its main parts. Imagine it as a team with three key players: an N-channel Enhancement MOSFET, a capacitor, and a high-precision operational amplifier. The MOSFET is like a switch, acting similar to a traffic light. It follows the orders of the input voltage through the drain and the control voltage through the gate. When it gets a positive control voltage pulse, it turns ON, becoming a closed switch. Conversely, when the control voltage is zero, it turns OFF, becoming an open switch.

(1m)

When the MOSFET is in the closed-switch state, the analog signal flows to the capacitor through the drain. The capacitor quickly charges to its highest level. But when the MOSFET opens, the charging stops. Thanks to the operational amplifier with its high impedance, the capacitor holds onto the charge, preventing it from disappearing. This holding period is crucial as it retains the sampled value.

(2m)

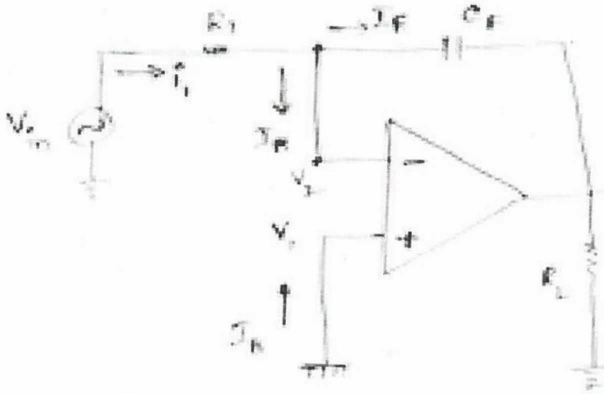


Since (-) terminal is at virtual ground, no current flows through $R_S$ and current through $R_f$. So $V_0 = -I_S R_f$.

**8.a .**

## Integrator

A circuit in which the output voltage waveform is the integral of input voltage waveform is the integrator (or) the integration amplifier is shown




$$V_0 = -\frac{1}{R_1 C_F}\int_0^t V_{in}\,dt + c$$

(2M)

Apply KCL at node $v_2$

$$i_1 = i_B + i_F$$

$\Rightarrow \quad i_1 \simeq I_F \quad$ (since $I_B$ is negligibly small)

$$\frac{V_{in} - V_2}{R_1} = C_F \frac{d}{dt}(v_2 - v_0)$$

(1M)

Since $v_1 = v_2 = 0$ then integrate with respect to time on both sides

$$\int_0^t \frac{V_{in}}{R_1}\,dt = \int_0^t C_F \frac{d}{dt}(-v_0)\,dt$$

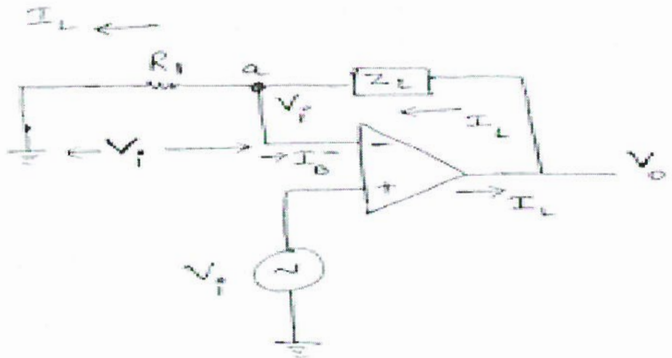
$$= C_F(-v_0) + v_0\big|_{t=0}$$

$$v_0 = -\frac{1}{R_1 C_F}\int_0^t v_{in}\,dt + c$$

where $c$ is integration constant and is proportional to $V_0$ at $t = 0$.

**7.b.**

V-I converter with floating load




(2m)

here the load $Z_L$ is floating.
at node 'a', $v_i = i_L R_1$ ($\because I_B^- = 0$)

$\Rightarrow i_L = v_i / R_1$

hence input voltage $v_i$ is converted to output current of $v_i/R_1$
Same current flows through signal source and load.

(1m)

Since the op-amp is used in non-inverting mode, the gain of the circuit is

$$1 + \frac{R}{R} = 2$$

the output voltage is

$$V_o = 2V_1 = V_i + V_o - i_L R$$

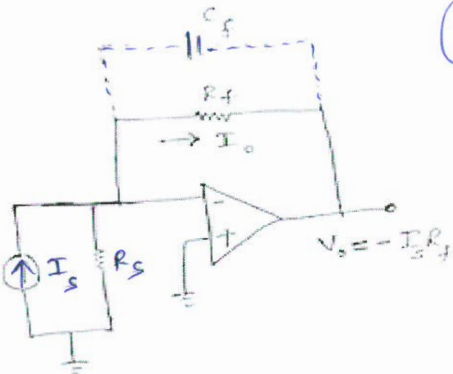
$$\Rightarrow v_i = i_L R$$

$$\Rightarrow i_L = \frac{v_i}{R}$$

Current to voltage converter (I to V converter)

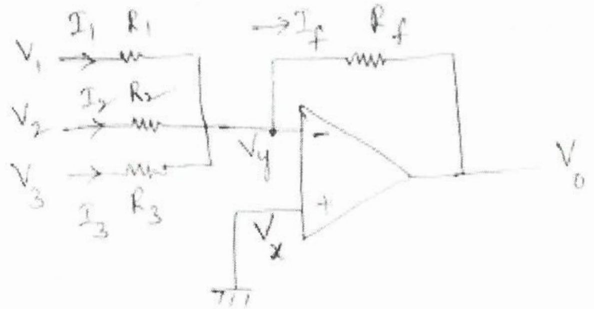
(2m)

Also called Transresistance Amplifier. photo diode, photo cell, photovoltaic cell give output current that is proportional to an incident radiation energy or light.
The current through these devices can be converted to voltage by using I to V converter and thereby amount of light on the photo device can be measured.



7.a.

## Inverting Adder




(3M)

Analysis: Apply KCL at node 'y'

$$I_1 + I_2 + I_3 = I_f$$

$$\frac{V_1 - V_y}{R_1} + \frac{V_2 - V_y}{R_2} + \frac{V_3 - V_y}{R_3} = \frac{V_y - V_0}{R_f}$$

(2M)

Since $V_x = 0 \Rightarrow V_y = 0$ (Due to Virtual ground)

$$\frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3} = \frac{0 - V_0}{R_f}$$

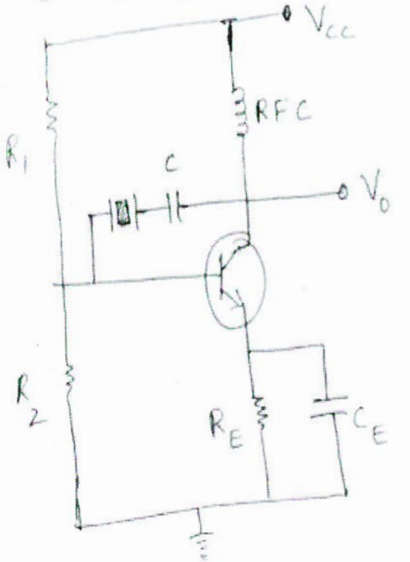
$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_f}$$

$$\Rightarrow V_0 = -\frac{R_f}{R_1}(V_1 + V_2 + V_3)$$

from above analysis, If $R_1 = R_2 = R_3 = R_f = R$

Then $V_0 = -(V_1 + V_2 + V_3)$

Crystal oscillator circuit




(1m)

the Crystal is Connected as a series element in feed back path from collector to base. The resistor $R_1$ $R_2$ and $R_E$ provide a voltage divider stabilized dc bias circuit.

Capacitor $C_E$ provides a ac bypass of the emitter resistor

RFC (radio frequency choke) provides for dc bias

The circuit frequency of oscillation is set by the series resonant frequency of a crystal and its value is given by

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$f_o$ does not effected by Suply voltage, transistor device parameters due to presence of a crystal.

**6.b.**

**Given:**

- $R = 6\,k\Omega = 6000\,\Omega$
- $C = 46\,nF = 46 \times 10^{-9}\,F$

(1m)

The frequency of a wien bridge oscillator is

(2m)

$$f_0 = \frac{1}{2\pi RC}$$

$$f_0 = \frac{1}{2 \times \pi \times 6000 \times 46 \times 10^{-9}}$$

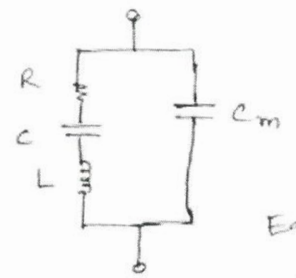
(2m)

$$f_0 = \frac{1}{2 \times 3.1416 \times 6000 \cdot 46 \times 10^{-9}} = \frac{1}{1.734 \times 10^{-3}} \approx \boxed{576.8\,\text{Hz}}$$

If an ac voltage is applied, the crystal starts vibrates at the frequency of applied voltage.

However, if the frequency of applied voltage is made equal to the natural frequency of a crystal, resonance takesplace and crystal vibrations reach a maximum value. This natural frequency is almost constant.

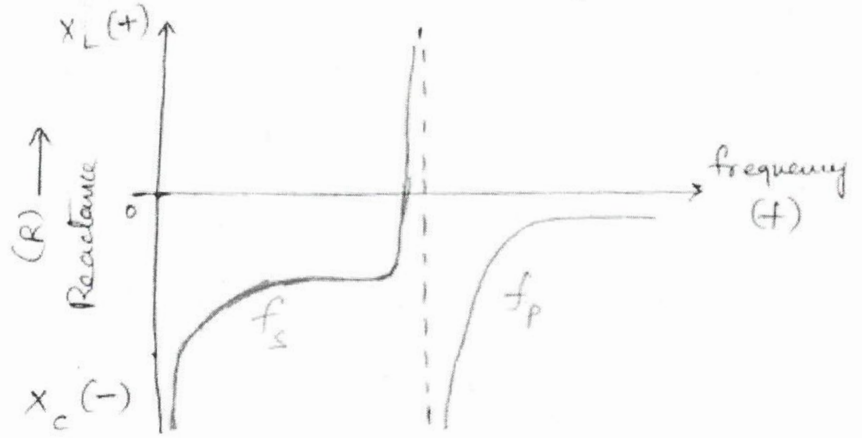
fig- Symbol of a Crystal




Equivalent circuit of a Crystal

(2m)

The frequency response of a crystal is shown below




(1m)

here, the crystal has two closely spaced resonant frequencies → Series resonant frequency ($f_s$)
→ parallel " " ($f_p$)

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$ & $$f_p = \frac{1}{2\pi\sqrt{LC_T}}$$ where $C_T = \left(\frac{CC_m}{C+C_m}\right)$

Value of $C_m$ is usually very large as compared to C.

Therefore value of $C_T \simeq C$

hence $f_s \simeq f_p$.

5

Given $R_s = 1\ k\Omega$ and $R_L = 1\ k\Omega$

**5.**

(a) Current gain, $$A_i = \frac{h_{fe}}{1 + h_{oe} \times R_L}$$

$$= \frac{50}{1 + 25 \times 10^{-6} \times 1 \times 10^{3}} = 48.78$$

(5m)

(b) Voltage gain, $$A_V = \frac{-h_{fe}}{\left(h_{oe} + \frac{1}{R_L}\right) Z_{in}}$$

(5m)

Here, $$Z_{in} = h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \frac{1}{R_L}}$$

$$= 1000 - \frac{2 \times 10^{-4} \times 50}{25 \times 10^{-6} + 1 \times 10^{-3}} = 990.24\ \Omega$$

Therefore, $$A_V = \frac{-50}{(25 \times 10^{-6} + 1 \times 10^{-3}) \times 990.24} = -49.26$$

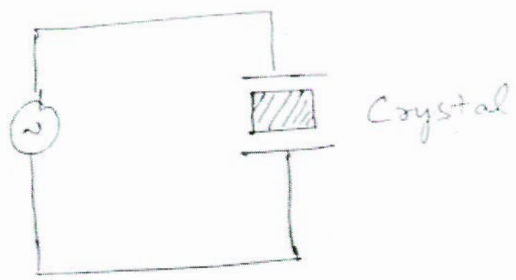
The output voltage is 180° out of phase to the input signal with a gain of 49.26.

**6.a.**

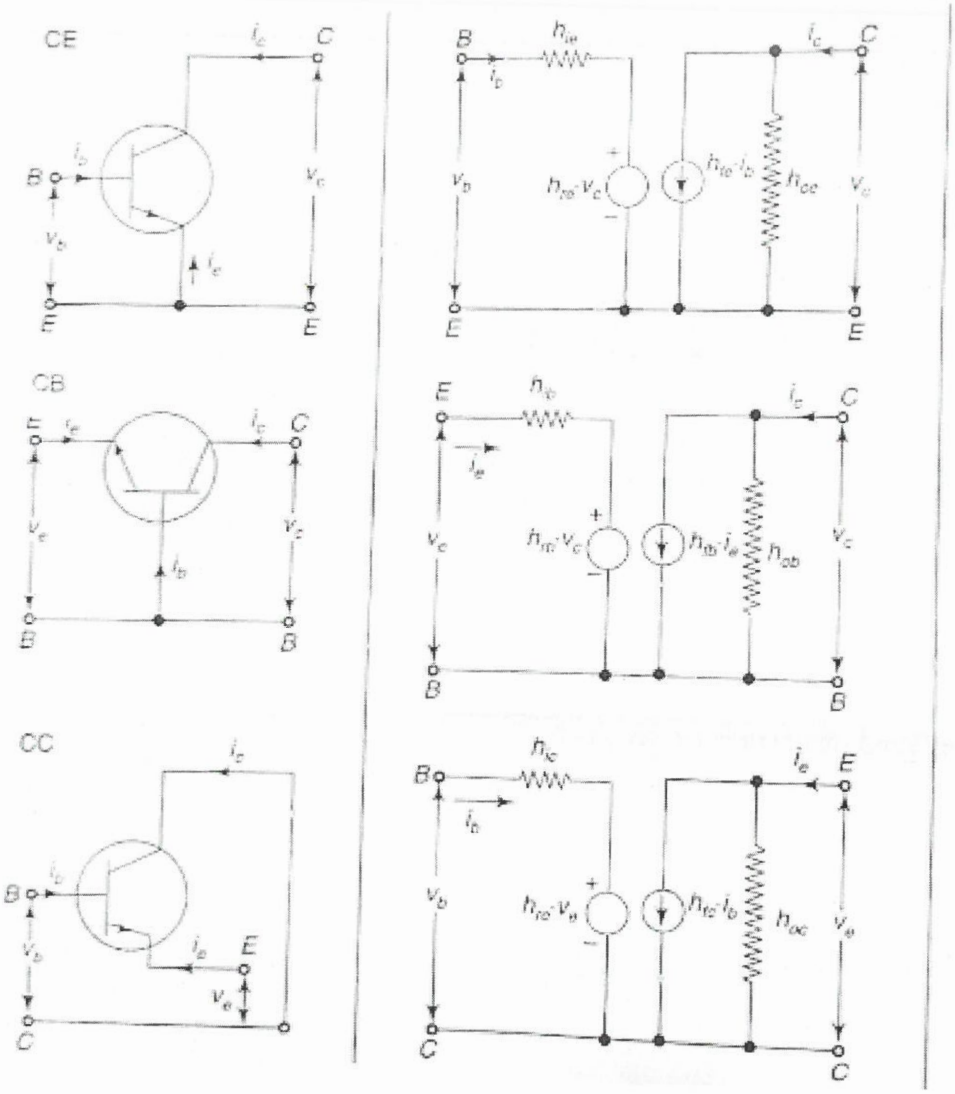
Working of a Quartz Crystal

Inorder to make a crystal work in an electronic circuit, the crystal is placed between two metal plates in the form of a capacitor and the ac voltage is applied in parallel to the crystal.

(1m)



**4.b.**




$v_b = h_{ie} \cdot i_b + h_{re} \cdot v_c$
$i_c = h_{fe} \cdot i_b + h_{oe} \cdot v_c$

$v_e = h_{ib} \cdot i_e + h_{rb} \cdot v_c$
$i_c = h_{fb} \cdot i_e + h_{ob} \cdot v_c$

(2M)

$v_b = h_{ic} \cdot i_b + h_{rc} \cdot v_e$
$i_e = h_{fc} \cdot i_b + h_{oc} \cdot v_e$

(3M)

*Conversion formulae for hybrid parameters*

| CE to CC | CE to CB |
|---|---|
| $h_{ic} = h_{ie}$ | $h_{ib} = \dfrac{h_{ie}}{1+h_{fe}}$ |
| $h_{rc} = 1$ | $h_{rb} = \dfrac{h_{ie}\,h_{oe}}{1+h_{fe}} - h_{re}$ |
| $h_{fc} = -(1+h_{fe})$ | $h_{fb} = \dfrac{-h_{fe}}{1+h_{fe}}$ |
| $h_{oc} = h_{oe}$ | $h_{ob} = \dfrac{h_{oe}}{1+h_{fe}}$ |

$$Z_i = h_i - \frac{h_f}{1+h_o Z_L} h_r Z_L$$

$$= h_i - \frac{h_f h_r}{Z_L\left(\frac{1}{Z_L}+h_o\right)} Z_L$$

Taking the load admittance as $Y_L = \frac{1}{Z_L}$

$$Z_i = h_i - \frac{h_f h_r}{Y_L + h_o}$$

Voltage Gain or Voltage Amplification Factor, $A_V$

$$A_V = \frac{V_2}{V_1}$$

$$V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

Output Admittance. $Y_O$

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by $V_2$,

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \qquad (1)$$

With $V_s = 0$, by KVL in the input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \qquad (2)$$

$$I_1 (R_s + h_i) + h_r V_2 = 0$$

Hence, $\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$ (3m)

Substituting Eq. **2** in Eq. **1**, we get

$$\frac{I_2}{V_2} = h_f\left(\frac{-h_r}{R_s + h_i}\right) + h_o$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

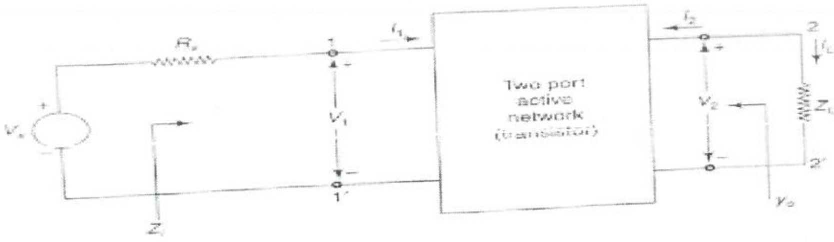
Note:- In above derivation, $h_i = h_{ie}$

$h_f = h_{fe}$

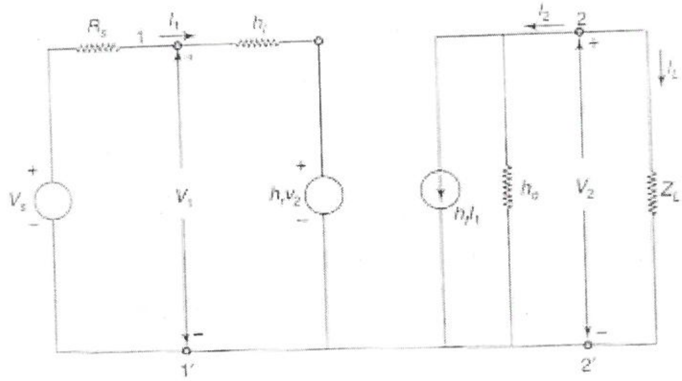
$h_o = h_{oe}$

$h_r = h_{re}$

4.a .




*Basic amplifier circuit*



In this,
$V_1 = V_b$ , $V_2 = V_c$
$i_1 = i_b$ , $i_2 = i_c$
for CE configuration.

(2m)

*transistor replaced by its hybrid model*

### Current Gain or Current Amplification, $A_I$

For a transistor amplifier, the current gain $A_I$ is defined as the ratio of output current to input current, i.e.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $\quad V_2 = I_L Z_L = -I_2 Z_L,$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1 + Z_L h_o) = h_f I_1$$

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}$$

Therefore,

$$A_I = \frac{-h_f}{1 + h_o Z_L}$$

$$Z_i = \frac{V_1}{I_1}$$

$$V_1 = h_i I_1 + h_r V_2$$

$$Z_i = \frac{h_i I_1 + h_r V_2}{I_1}$$

**Input Impedance**

3.b

Thevenin voltage at base:

$$V_T = V_{TH} = V_{CC} \cdot \frac{R_2}{R_1 + R_2} = 23 \cdot \frac{10}{90 + 10} = 23 \cdot 0.1 = 2.3\,V$$

Thevenin resistance:

$$R_B = R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{90 \cdot 10}{90 + 10} = \frac{900}{100} = 9\,k\Omega$$

$$V_T = \frac{I_C}{\beta} R_B + V_{BE} + \left(\frac{I_C}{\beta} + I_C\right) R_E$$ (3 m)

**$R_E$ value is not given in problem , it may be assumed as any value and it may be considered**

Let $R_E = 1\ k\Omega$

$$2.3 = \frac{I_C}{55} \cdot 9000 + 0.6 + \left(\frac{I_C}{55} + I_C\right) \cdot 1000$$

$$I_C = 1.44\,\text{mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 23 - 1.44 \cdot (12 + 1) = 23 - 1.44 \cdot 13 = 23 - 18.72 = \boxed{4.28\,\text{V}}$$

**Operating Point:**

$$\boxed{I_C = 1.44\,\text{mA}, \quad V_{CE} = 4.28\,\text{V}}$$ (1m)

For self-bias:

$$S = \frac{1 + \beta}{1 + \beta \cdot \frac{R_E}{R_B}} = \frac{1 + 55}{1 + 55 \cdot \frac{1000}{9000}} = \frac{56}{1 + 6.111} = \frac{56}{7.111} \approx \boxed{7.87}$$ (1m)