	b)	The h-parameters of a transistor used in a common emitter circuit are hie=1kΩ, hre=10 x 10^{-4}, hfe=50, hoe=25×10^{-6}. The load resistance for the transistor is 1 kΩ in the collector circuit. Determine A_i, A_v, R_i and R_o in the amplifier stage (Assume Rs=1000Ω)	L3	CO4	5 M
		UNIT-V			
10	a)	Explain the constructional features of a depletion mode P-channel and explain its basic operation.	L2	CO4	5 M
	b)	Explain the drain characteristics and transfer characteristics of a JFET.	L2	CO4	5 M
		OR			
11	a)	Summarize Small Signal Model of JFET.	L2	CO4	5 M
	b)	With neat diagrams, explain the circuit and small-signal analysis of a Common Gate (CG) amplifier.	L2	CO4	5 M

PVP 23

Code: 23EC3301

II B.Tech - I Semester – Regular / Supplementary Examinations
NOVEMBER 2025

ELECTRONIC DEVICES AND CIRCUITS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

PART – A

		BL	CO
1.a)	Define Drift and diffusion currents.	L1	CO1
1.b)	Differentiate between avalanche breakdown and Zener breakdown.	L3	CO2
1.c)	What is a clamping circuit? Mention any two applications.	L1	CO2
1.d)	What is the need of rectifier? List different types of rectifiers.	L1	CO2
1.e)	Write the relation between α and β of a transistor.	L1	CO3
1.f)	Why is bias compensation necessary?	L1	CO3
1.g)	Give the approximate h-parameter conversion formulae for CB configuration in terms of CE.	L1	CO4
1.h)	Write the limitations of h-parameters.	L1	CO4
1.i)	Compare JFET and BJT.	L3	CO4
1.j)	What is the condition for pinch-off in JFET?	L1	CO4

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	How does the reverse saturation current of diode varies with temperature? Explain.	L2	CO2	5 M
	b)	Derive the expression for transition capacitance C_T of a diode.	L4	CO2	5 M
		OR			
3	a)	Define tunneling phenomenon. Explain the working of a tunnel diode with energy band diagram.	L2	CO2	5 M
	b)	With neat diagram, explain how a UJT can be used as a relaxation oscillator.	L2	CO2	5 M
		UNIT-II			
4	a)	Explain the operation of series and shunt clipping circuits with neat diagrams.	L2	CO2	5 M
	b)	Derive the expressions for the following parameters of the halfwave rectifier circuit: i) Average d.c current (I_{DC}) ii) Average d.c voltage (V_{DC}) iii) D.C power output (P_{DC}) iv) A.C input power (P_{AC})	L4	CO2	5 M
		OR			
5	a)	A 230V, 60Hz voltage is applied to the primary of a 5:1 step down center tapped transformer used in the full wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω, determine : i) DC voltage across the load ii) DC current flowing to the load iii) DC power delivered to the load iv) PIV across each diode.	L3	CO2	5 M
	b)	Draw and explain the circuit diagram of full wave rectifier with L-section filter.	L2	CO2	5 M
		UNIT-III			
6	a)	With neat diagrams, explain the input and output characteristics of CB configurations.	L2	CO3	5 M
	b)	Compare CB, CE and CC transistor configurations.	L3	CO3	5 M
		OR			
7	a)	What is transistor biasing? Explain the need for biasing in transistor amplifiers.	L2	CO3	5 M
	b)	Design a voltage divider bias networking using a supply of 24V, β=110 and I_{CQ}=4mA, V_{CEQ}=8V. Choose $V_E=V_{CC}/8$.	L3	CO3	5 M
		UNIT-IV			
8	a)	Analyze a single stage transistor amplifier using h-parameter	L4	CO4	5 M
	b)	Draw the circuit diagram of CC amplifier using hybrid parameter and derive the expressions for A_i, A_v, R_i and R_o.	L4	CO4	5 M
		OR			
9	a)	Derive the expressions for A_i, A_v, R_i and R_o of CB amplifier using approximate model.	L4	CO4	5 M

II B.Tech - I Semester - Regular/Supplementary Examinations
NOVEMBER 2025
ELECTRONIC DEVICES AND CIRCUITS (23EC3301)
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours **Max. Marks:70**

PART A

1.a) Define Drift and diffusion currents.

Definition of Drift current -1M
Definition of diffusion current -1M

b) Differentiate between avalanche breakdown and Zener breakdown.

Any 2 comparisons-2M

c) What is a clamping circuit? Mention any two applications.

Definition -1M
Any 2 applications-1M

d) What is the need of rectifier? List different types of rectifiers.

Purpose-1M
Types-1M

e) Write the relation between α and β of a transistor.

Relation-2M

f) Why is bias compensation necessary?

Reason-2M

g) Give the approximate h-parameter conversion formulae for CB configuration in terms of CE.

Approximate h-parameter conversion formulae-2M

h) Write the limitations of h-parameters.

Any 2 Limitations-2M

i) Compare JFET and BJT.

Any 2 comparisons-2M

j) What is the condition for pinch-off in JFET?

Condition-2M

PART B

UNIT I

2.a) How does the reverse saturation current of diode vary with temperature? Explain. -5M

Daigram -2M **Explanation -3M**

b) Derive the expression for transition capacitance C_T of a diode. -5M

Expression -5M

(OR)

3.a) Define tunneling phenomenon. Explain the working of a tunnel diode with energy band diagram. -5M

Definition-1M Diagram -2M Working -2M

b) With neat diagram, explain how a UJT can be used as a relaxation oscillator. -5M

Diagram -2M Explanation -3M

(OR)

4.a) Explain the operation of series and shunt clipping circuits with neat diagrams. -5M

Diagram -2M Operation of series and shunt clipping circuits -3M

b) Derive the expressions for the following parameters of the half-wave rectifier circuit: -5M

i) Average d.c current (I_{DC}) ii) Average d.c voltage (V_{DC})

iii) D.C power output (P_DC) iv) A.C input power (P_{AC})

i) Average d.c current (I_{DC}) -2M ii) Average d.c voltage (V_{DC}) -1M

iii) D.C power output (P_DC) -1M iv) A.C input power (P_{AC}) -1M

Unit II

5.a) A 230V, 60Hz voltage is applied to the primary of a 5:1 step-down center-tapped transformer used in the full-wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together have a resistance of 100Ω, determine: -5M

i) DC voltage across the load

ii) DC current flowing to the load

iii) DC power delivered to the load

iv) PIV across each diode

i) DC voltage across the load-2M ii) DC current flowing to the load-1M

iii) DC power delivered to the load-1M iv) PIV across each diode-1M

b) Draw and explain the circuit diagram of full-wave rectifier with L-section filter. -5M

Diagram -2M Explanation -3M

Unit III

6.a) With neat diagrams, explain the input and output characteristics of CB configurations. -5M

Diagram -2M Explanation -3M

b) Compare CB, CE and CC transistor configurations. -5M

Any 5 comparisons

(OR)

7.a) What is transistor biasing? Explain the need for biasing in transistor amplifiers. -5M

Definition -2M Purpose -3M

b) Design a voltage divider bias network using a supply of 24V, $\beta = 110$ and $I_{CQ} = 4mA$, $V_{CEQ} = 8V$. Choose $V_E = V_{CC/8}$. -5M

Solution -5M

Unit IV

8.a) Analyze a single stage transistor amplifier using h-parameter. -5M

Definition -2M Analyze -3M

b) Draw the circuit diagram of CC amplifier using hybrid parameter and derive the expressions for Ai, Av, Ri and Ro. -5M

Circuit diagram -2M Derivation -3M

9.a) Derive the expressions for Ai, Av, Ri and Ro of CB amplifier using approximate model. 5M

Ai-2M Av-1M, Ri-1M and Ro-1M

b) The h-parameters of a transistor used in a common emitter circuit are hie = 1 kΩ, hre = 10×10^{-4}, hfe = 50, hoe = 25×10^{-6}. The load resistance for the transistor is 1 kΩ in the collector circuit. Determine Ai, Av, Ri and Ro in the amplifier stage (Assume Rs = 1000 Ω) -5M

Solution -5M

Unit V

10.a) Explain the constructional features of a depletion mode P-channel and explain its basic operation. -5M

Features 2M Operation-3M

b) Explain the drain characteristics and transfer characteristics of a JFET. -5M

Drain characteristics-2M Transfer characteristics-3M

11 a) Summarize Small Signal Model of JFET. -5M

Summary-5M

b) With neat diagrams, explain the circuit and small-signal analysis of a Common Gate (CG) amplifier. -5M

Diagram -2M Explanation -3M

II B.Tech - I Semester - Regular/Supplementary Examinations

NOVEMBER 2025

ELECTRONIC DEVICES AND CIRCUITS (23EC3301)

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours **Max. Marks:70**

PART A

1.a) Define Drift and diffusion currents.

Sol:

DRIFT CURRENT :-

Drift current is the electric current, or movement of charge carriers, which is due to the applied electric field, often stated as the electromotive force over a given distance.

DIFFUSION CURRENT:-

Diffusion current is a current in a semiconductor caused by the diffusion of charge carriers. This is the current which is due to the transport of charges occurring because of nonuniform concentration of charged particles in a semiconductor.

b) Differentiate between avalanche breakdown and Zener breakdown.

Sol: **Any 2**

Zener Breakdown	Avalanche Breakdown
The process in which the electrons move across the barrier from the valence band of p-type material to the conduction band of n-type material is known as Zener breakdown.	The process of applying high voltage and increasing the free electrons or electric current in semiconductors and insulating materials is called an avalanche breakdown.
This is observed in Zener diodes having a Zener breakdown voltage V_z of 5 to 8 volts.	This is observed in Zener diode having a Zener breakdown voltage V_z greater than 8 volts.
The valence electrons are pulled into conduction due to the high electric field in the narrow depletion region.	The valence electrons are pushed to conduction due to the energy imparted by accelerated electrons, which gain their velocity due to their collision with other atoms.
The increase in temperature decreases the breakdown voltage.	The increase in temperature increases the breakdown voltage.
The VI characteristics of a Zener breakdown has a sharp curve.	The VI characteristic curve of the avalanche breakdown is not as sharp as the Zener breakdown.
It occurs in diodes that are highly doped.	It occurs in diodes that are lightly doped.

c) What is a clamping circuit? Mention any two applications.

Sol: A clamping circuit is an electronic circuit that shifts the DC level of a signal without changing the shape of its waveform. It moves the whole signal either up or down about the reference level.

Applications (Any 2)

- It is used as a voltage multiplier.
- It is used for improving the reverse recovery time.
- It is used for removing the distortion in the signal.
- It is also used as test equipment.

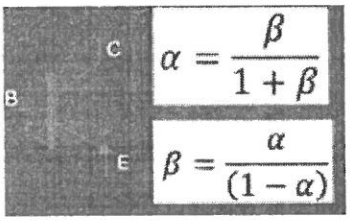
d) What is the need of rectifier? List different types of rectifiers.

Sol: A rectifier is needed to convert **alternating current (AC)** into **direct current (DC)**

Rectifiers are classified into two main types: half-wave and full-wave

e) Write the relation between α and β of a transistor.

Sol:



f) Why is bias compensation necessary?

Sol: Bias compensation is necessary to maintain stable circuit operation by countering the effects of temperature changes and component aging, which can otherwise cause a transistor's operating point to drift and lead to performance issues or failure

g) Give the approximate h-parameter conversion formulae for CB configuration in terms of CE.

Sol:

The approximate h-parameter conversion formulae for the common-base (CB) configuration in terms of common-emitter (CE) parameters are: $h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$,

$h_{rb} = \frac{h_{ie}h_{oe} - h_{re}}{1 + h_{fe}}$, $h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$, and $h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$.

h) Write the limitations of h-parameters.

Sol: **Any 2**

Frequency Dependence
Small-Signal Only
Measurement Difficulties
Bias-Point Dependency
Configuration Specificity

i) Compare JFET and BJT.

Sol: **Any 2**

S.No	BJT	JFET
1	Low input impedance	High input impedance
2	High output impedance	Low output impedance
3	Bipolar device	Unipolar device
4	Noise is more	Less noise
5	Cheaper	Costlier
6	Gain is more	Less gain
7	Current controlled device	Voltage controlled device

j) What is the condition for pinch-off in JFET?

Sol: Pinch-off in a JFET occurs when the drain-to-source voltage (V_{DS}) exceeds the pinch-off voltage (V_P) while the gate-to-source voltage (V_{GS}) is held constant

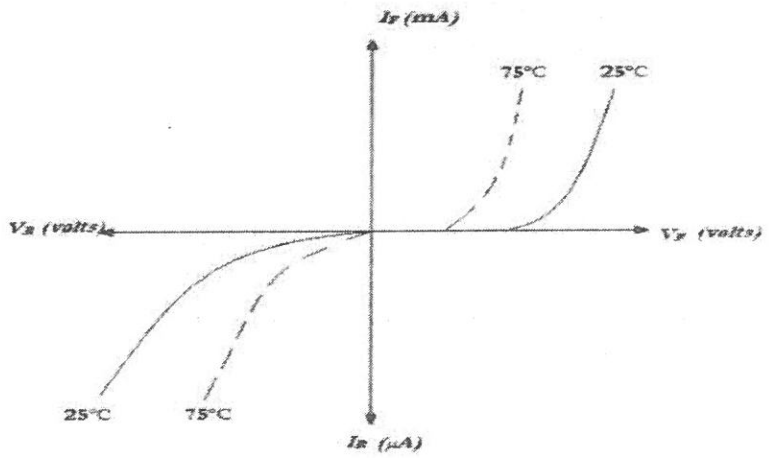
PART B

UNIT 1

2.a) How does the reverse saturation current of diode vary with temperature? Explain. -5M

Sol:

- In forward bias, **current flows easily** (positive to p-side, negative to n-side).
- As temperature goes up, the diode allows **more current** to flow for the **same voltage**.
  - Like: At higher heat, the diode gets "more active."
- Normally, a silicon diode needs about **0.7 V** to start conducting.
  - But if temperature increases, it might need only **0.6 V or less**.
    - So, the diode **turns on earlier** at high temperature.
- **V-I graph**
  - The **graph shifts left**
  - For the **same voltage**, we get **more current**



Effect of Temperature on Forward Bias

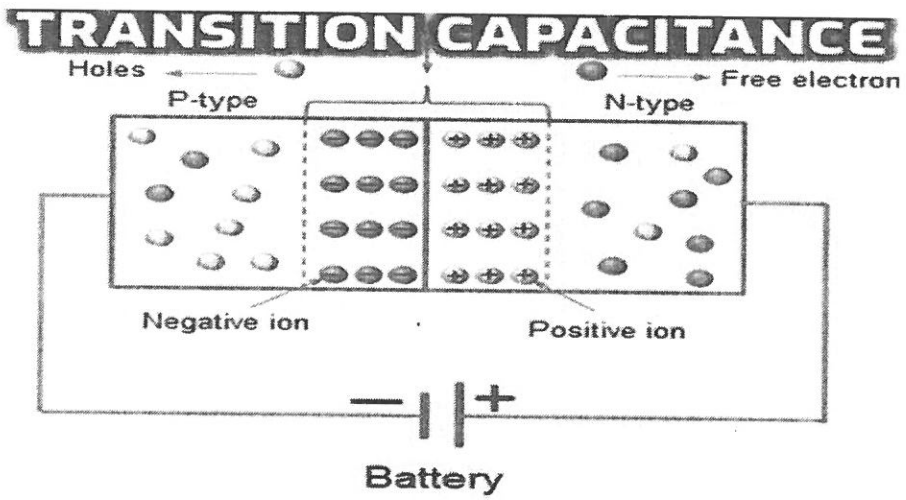
- In reverse bias, the diode is connected in a way that **stops current** (positive to n-side, negative to p-side).
- Only a **tiny current** flows — this is called **leakage current** or **reverse saturation current Is**
- As temperature goes up, more minority carriers (like stray electrons or holes) are available.
    - This cause **more reverse current** to flow.
        - So, even though the diode is supposed to block current, a little more "leaks" through when it gets hot.

b) Derive the expression for transition capacitance C_T of a diode. -5M

Sol:

Transition Capacitance (CT).

- Applicable in Reverse bias
- Also called space charge capacitance
- When a P-N junction is subjected to reverse bias, the depletion zone behaves like an insulating layer or dielectric, while the adjacent p-type and n-type regions, which have low resistance, function as the capacitor's plates.
- This setup allows the P-N junction to be modeled as a parallel plate capacitor.
- Applying reverse bias pushes the majority charge carriers away from the junction, causing the depletion region's width, denoted as (W), to expand.



Transition Capacitance

- The amount of capacitance changed with increase in voltage is called transition capacitance.
- The transition capacitance is also known as depletion region capacitance, junction capacitance or barrier capacitance.
- Transition capacitance is denoted as C_T.
- The change of capacitance at the depletion region can be defined as the change in electric charge per change in voltage.
- $CT = dQ / dV$ Where,

  CT = Transition capacitance

  dQ = Change in electric charge

  dV = Change in voltage
- The transition capacitance can be mathematically written as,

  $C_T = \varepsilon A / W$ Where,

  ε = Permittivity of the semiconductor

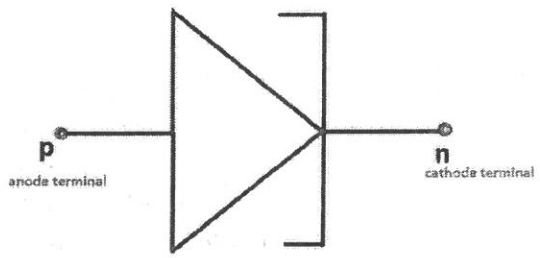
  A = Area of plates or p-type and n-type regions

  W = Width of depletion region

3.a) Define tunneling phenomenon. Explain the working of a tunnel diode with energy band diagram.

Sol: The tunnel diode, also known as the Esaki diode, was introduced by Leo Esaki.

- A **Tunnel Diode** is a **heavily doped** p-n junction diode that shows a special behavior:
  - When voltage increases, current **first increases**, then **decreases**, and later **increases again**.
  - This decrease in current with increase in voltage is called **Negative Resistance**.



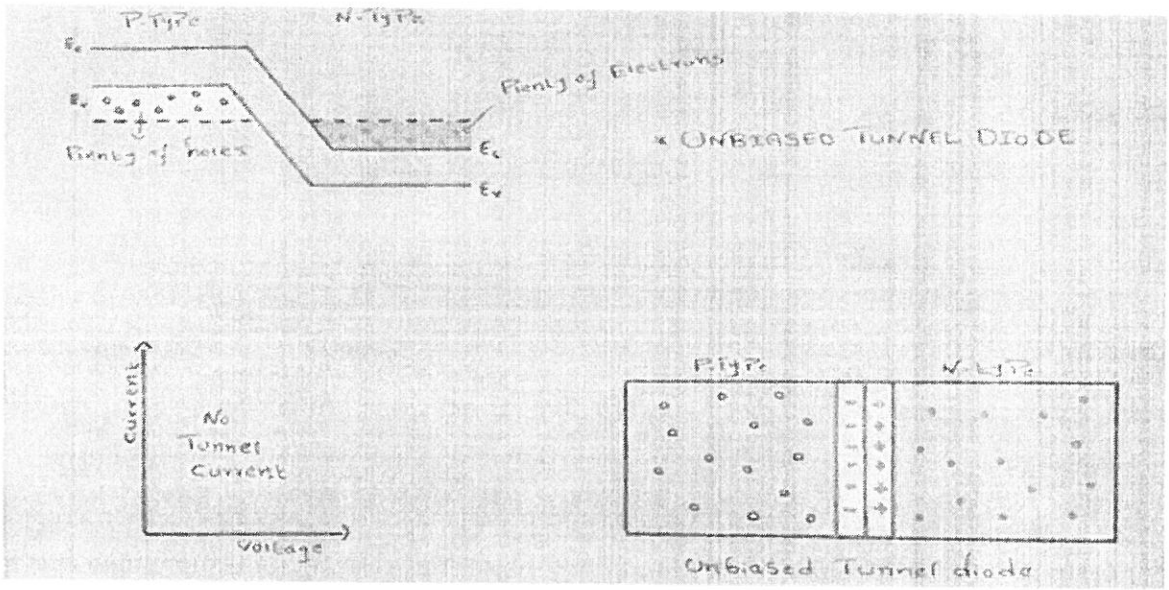
Symbol of Tunnel diode

Working of Tunnel Diode

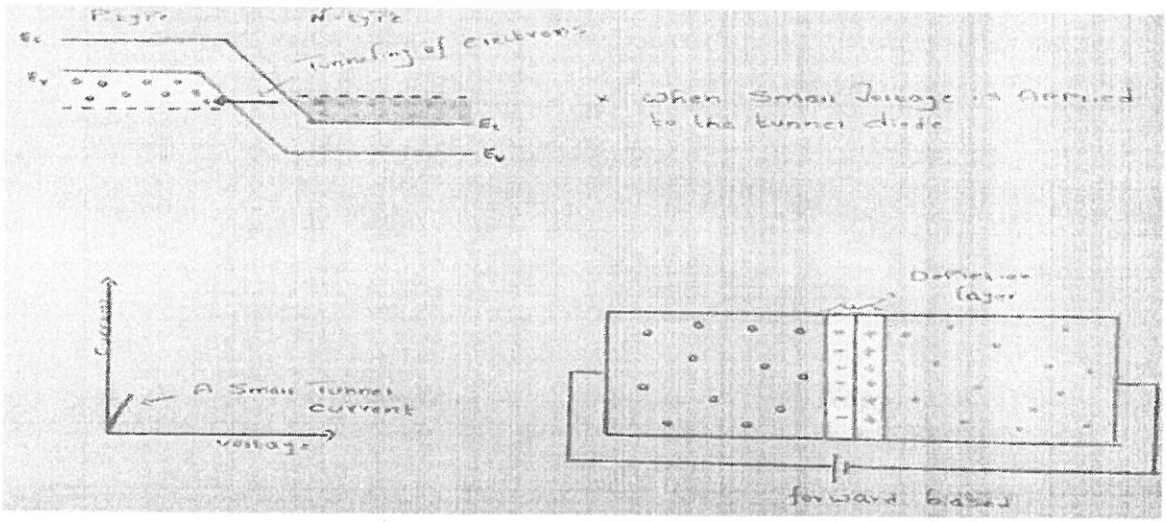
- The operation of tunnel diode depends on the quantum mechanics principle known as **Tunneling**.
- In electronics, tunneling means a direct flow of electrons across the small depletion region without any force.
- The germanium material is commonly used to make the tunnel diodes.

- Less preferable materials are gallium arsenide, gallium antimonide, and silicon.

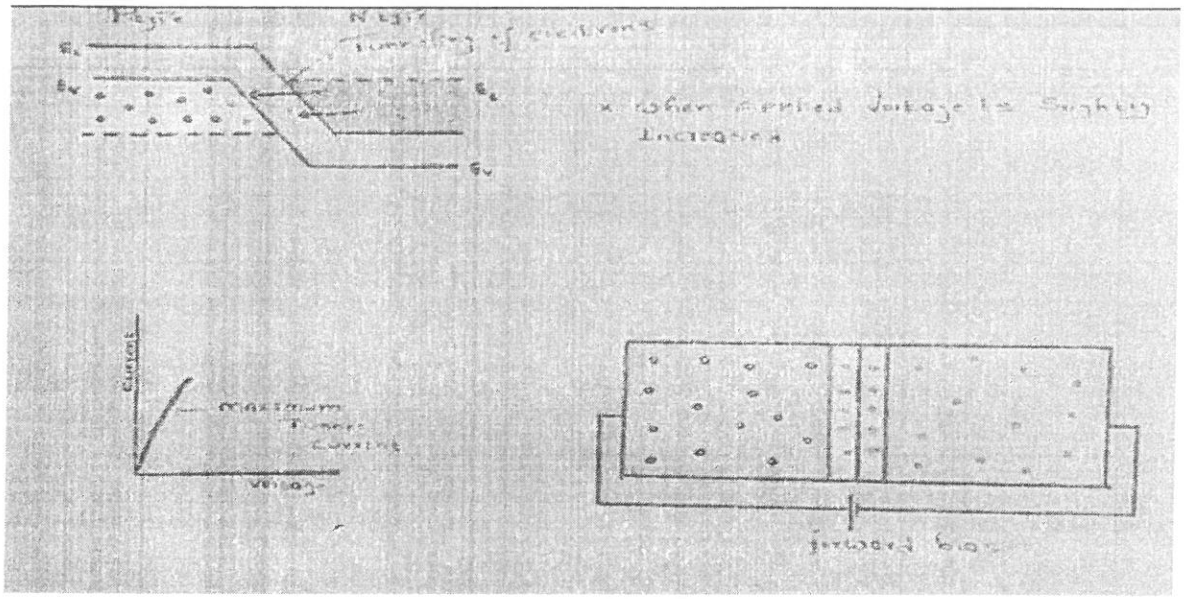
- In tunnel diode, the p-type and n-type semiconductor is heavily doped which means a large number of impurities are introduced into the p-type and n-type semiconductor.
  - This heavy doping process produces an extremely narrow depletion region



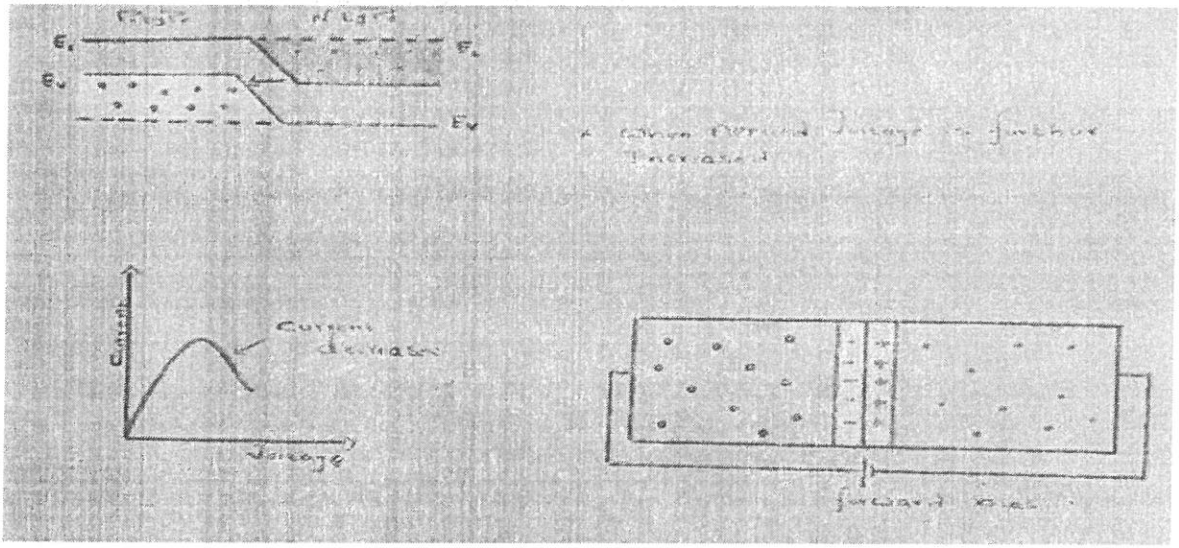
Because of equal number of electrons and holes movement from one junction to another, the net current will be zero



In this condition some of the electron of conduction band of n-type tunnel in empty valence band of p-type, this creates a small current flow through the diode.



Because of the increase in voltage the over lapping is increased. Energy level of conduction band of n-type is exactly equal to the energy level of valence band at p-type result maximum tunnel current flow.



When we further increase the voltage more than the peak voltage, the energy level of conduction band at n-side and the valence band at p-side misalign. Due to this misalignment tunneling of charge carrier decreases, as result decrease in tunnel current

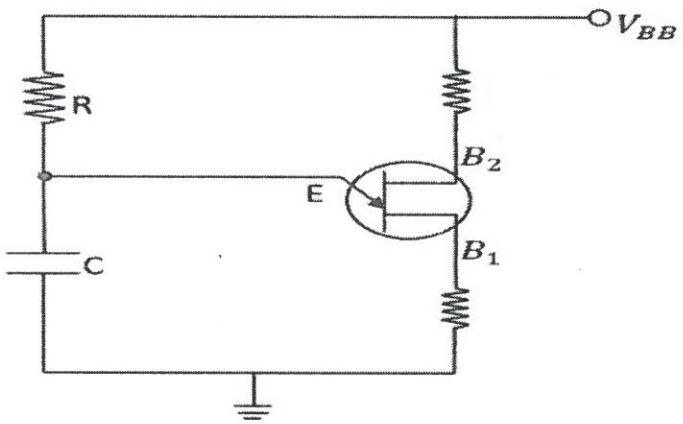
b) With neat diagram, explain how a UJT can be used as a relaxation oscillator. -5M

Sol: An oscillator is a device that produces a waveform by its own, without any input. Though some dc voltage is applied for the device to work, it will not produce any waveform as input. A relaxation oscillator is a device that produces a non-sinusoidal waveform on its own. This waveform depends generally upon the charging and discharging time constants of a capacitor in the circuit.

Construction and Working

The emitter of UJT is connected with a resistor and capacitor as shown. The RC time constant determines the timings of the output waveform of the relaxation oscillator. Both the bases are connected with a resistor each. The dc voltage supply VBB is given.

The following figure shows how to use a UJT as a relaxation oscillator.



Initially, the voltage across the capacitor is zero.

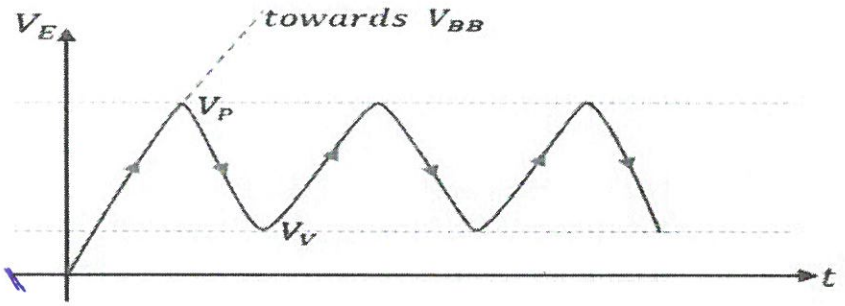
$$Vc=0$$

The UJT is in OFF condition. The resistor R provides a path for the capacitor C to charge through the voltage applied.

The capacitor charges according to the voltage

$$V=V_0(1-e^{-t/RC})$$

The capacitor usually starts charging and continues to charge until the maximum voltage VBB. But in this circuit, when the voltage across capacitor reaches a value, which enables the UJT to turn ON (the peak voltage) then the capacitor stops to charge and starts discharging through UJT. Now, this discharging continues until the minimum voltage which turns the UJT OFF (the valley voltage). This process continues and the voltage across the capacitor, when indicated on a graph, the following waveform is observed.



So, the charge and discharge of capacitor produces the sweep waveform as shown above. The charging

time produces increasing sweep and the discharging time produces decreasing sweep. The repetition of this cycle forms a continuous sweep output waveform.

As the output is a non-sinusoidal waveform, this circuit is said to be working as a relaxation oscillator.

UNIT II

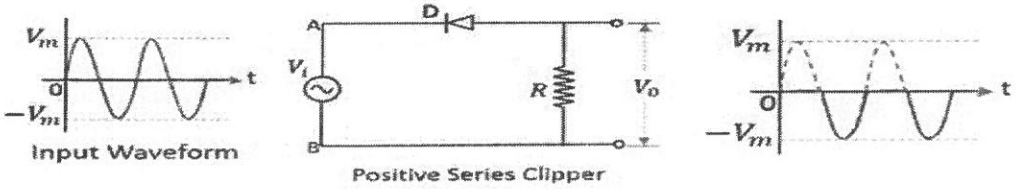
4.a) Explain the operation of series and shunt clipping circuits with neat diagrams. -5M

Sol: **Any 1 from series clipping circuits -2.5Marks**

Any 1 from shunt clipping circuits -2.5Marks

Unbiased Positive clippers

- A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Series Clipper.**



Positive Half-Cycle

Point A is **positive** w.r.t. Point B.

Diode reverse biased → acts like an **open switch.**

No current flows ,hence V_o=0.

Negative Half-Cycle

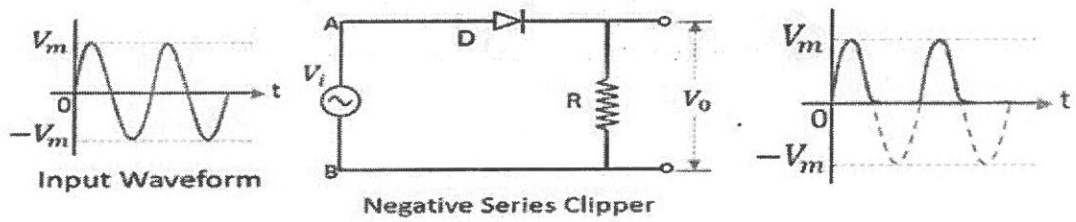
Point A is **negative** w.r.t. Point B.

Diode forward biased ,then diode acts like a **closed switch.**

Input voltage appears fully across the load i.e. V_o equals input.

Unbiased Negative clippers

- A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper.**



Positive Half Cycle

Point A is positive compared to point B.

Diode is **forward biased** , it acts like a **closed switch.**

Input voltage appears fully across the load i.e. V_o equals input.

Negative Half Cycle

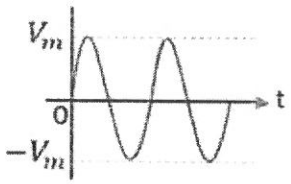
Point A is negative compared to point B.

Diode is **reverse biased**, it acts like an **open switch.**

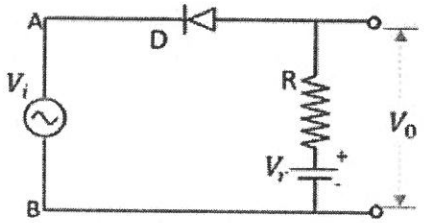
No current flows ,hence V_o=0.

Positive Series Clipper with positive Vr

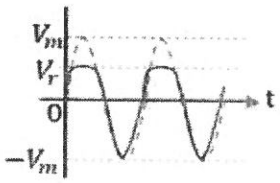
- Clipper where the diode is in series with the input and given a positive reference voltage Vr, so it clips the positive parts of the waveform above Vr.



Input Waveform



Positive Series Clipper with positive V_r

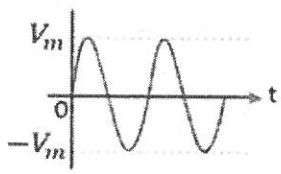


Practical Output Waveform

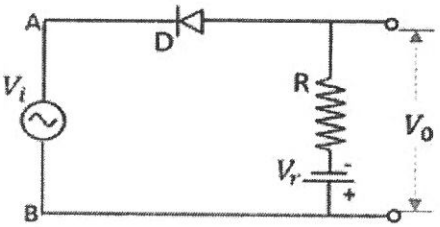
- **During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output.**
- **During its negative cycle, the diode gets forward biased and conducts like a closed switch. Hence the output waveform appears as shown in the above figure.**

Positive Series Clipper with negative Vr

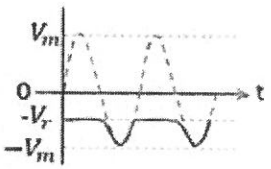
- A clipper where the diode is connected in series with the input and given a negative reference voltage Vr, so it cuts the positive parts of the waveform above a set negative level.



Input Waveform



Positive Series Clipper with negative V_r

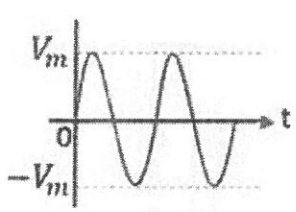


Practical Output Waveform

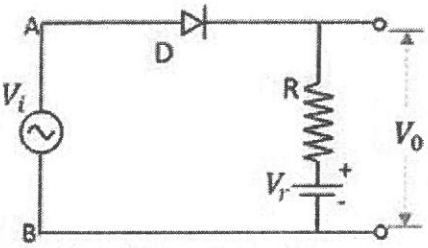
- **During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output. As the reference voltage is negative, the same voltage with constant amplitude is shown.**
- **During its negative cycle, the diode gets forward biased and conducts like a closed switch. Hence the input signal that is greater than the reference voltage, appears at the output.**

Negative Series Clipper with positive Vr

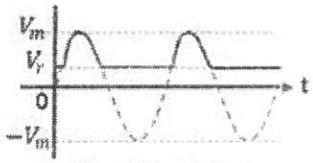
- A Clipper circuit in which the diode is connected in series to the input signal and biased with positive reference voltage Vr and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper with positive Vr**



Input Waveform



Negative Series Clipper with positive V_r

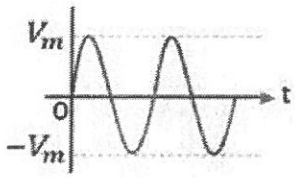


Practical Output Waveform

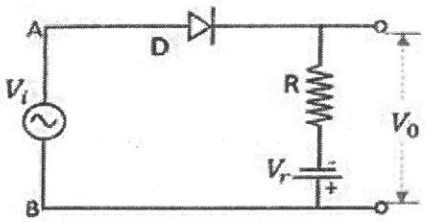
During the positive cycle of the input, the diode starts conducting only when the anode voltage value exceeds the cathode voltage value of the diode.
During the negative half cycle, as the diode gets reverse biased and the loop gets completed, no output is present.

Negative Series Clipper with negative Vr

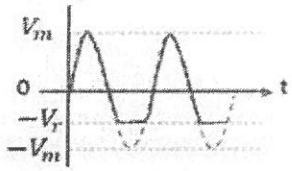
- A Clipper circuit in which the diode is connected in series to the input signal and biased with negative reference voltage Vr and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper with negative Vr.**



Input Waveform



Negative Series Clipper with negative V_r



Practical Output Waveform

- **During the positive cycle of the input the diode gets forward biased and the input signal appears at the output.**
- **During its negative cycle, the diode gets reverse biased and hence will not conduct. But the negative reference voltage being applied, appears at the output. Hence the negative cycle of the output waveform gets clipped after this reference level.**

Positive Shunt Clipper

A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper**

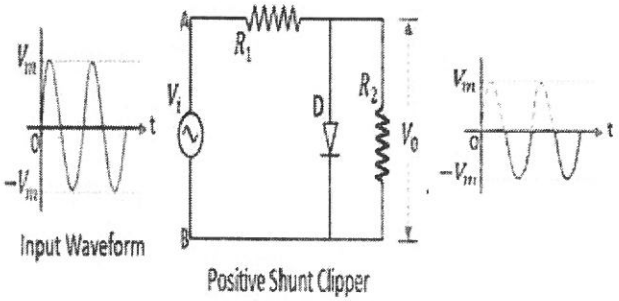
Positive Shunt Clipper – Working

Positive Half-Cycle

Point A is **positive** w.r.t. Point B.
Diode forward biased → acts like a **closed switch.**
Output voltage (V_0) = **0 V** (clipped).

Negative Half-Cycle

Point A is **negative** w.r.t. Point B.
Diode reverse biased → acts like an **open switch.**
Output voltage (V_0) = **same as input** (unchanged).



Negative Shunt Clipper

- A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the negative portions of the waveform, is termed as **Negative Shunt Clipper.**

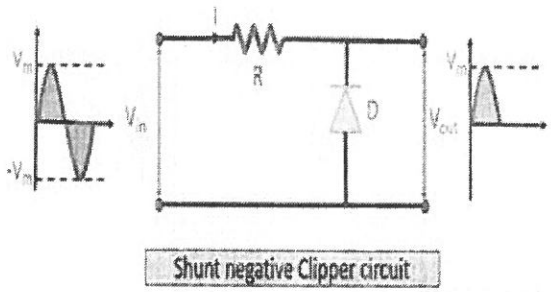
Negative Shunt Clipper – Working

Positive Half-Cycle

Point A is **positive** w.r.t. Point B.
Diode reverse biased it acts like an **open switch.**
Output voltage (V_0) = **same as input** (unchanged).

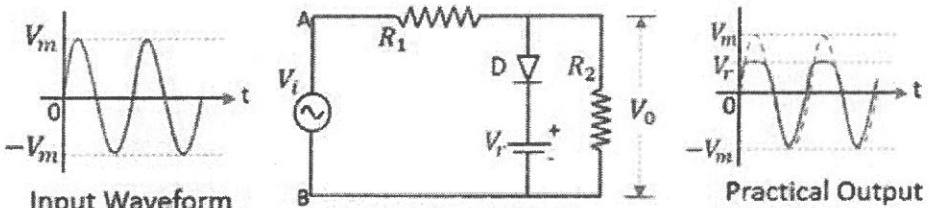
Negative Half-Cycle

Point A is **negative** w.r.t. Point B.
Diode forward biased → acts like a **closed switch.**
Output voltage (V_0) = **0 V** (clipped).



Positive Shunt Clipper with positive Vr

- A clipper where the diode is connected in parallel to the input and given a positive reference voltage Vr, so it cuts off the positive parts of the waveform above Vr.



Input Waveform

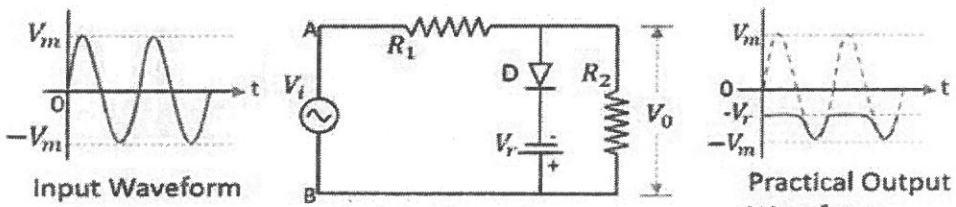
Positive Shunt Clipper with positive V_r

Practical Output Waveform

During the positive cycle of the input the diode gets forward biased and nothing but the reference voltage appears at the output.
During its negative cycle, the diode gets reverse biased and behaves as an open switch. The whole of the input appears at the output.

Positive Shunt Clipper with negative Vr

- A clipper where the diode is connected in parallel to the input and given a negative reference voltage Vr, so it clips the positive parts of the waveform above a set negative level.



Input Waveform

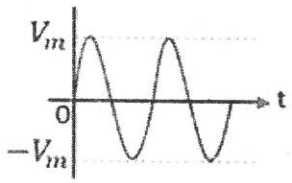
Positive Shunt Clipper with negative V_r

Practical Output Waveform

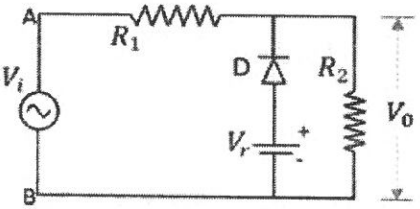
- During the positive cycle of the input, the diode gets forward biased and the reference voltage appears at the output. As the reference voltage is negative, the same voltage with constant amplitude is shown.
- During its negative cycle, the diode gets reverse biased and behaves as an open switch. Hence the input signal that is greater than the reference voltage, appears at the output.

Negative Shunt Clipper with positive Vr

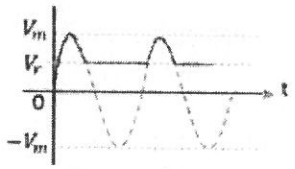
- A clipper where the diode is connected in parallel to the input and given a positive reference voltage Vr, so it clips the negative parts of the waveform below a set positive level.



Input Waveform



Negative Shunt Clipper with positive V_r

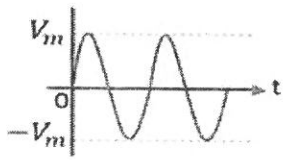


Practical Output Waveform

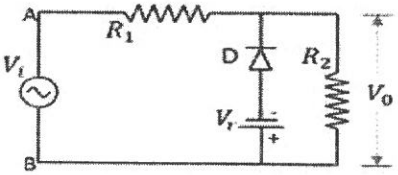
- During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, which is greater than the reference voltage applied, appears at the output. The signal below reference voltage level gets clipped off.
- During the negative half cycle, as the diode gets forward biased and the loop gets completed, no output is present.

Negative Shunt Clipper with negative Vr

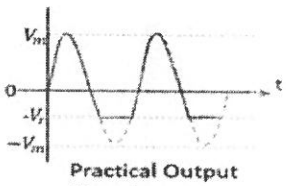
- A clipper where the diode is connected in parallel to the input and given a negative reference voltage Vr, so it clips the negative parts of the waveform below Vr.



Input Waveform



Negative Shunt Clipper with negative V_r



Practical Output Waveform

- During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, appears at the output Vo.
- During the negative half cycle, the diode gets forward biased. The negative voltage up to the reference voltage, gets at the output and the remaining signal gets clipped off.

b) Derive the expressions for the following parameters of the half-wave rectifier circuit: -5M

i) Average d.c current (I_{DC}) ii) Average d.c voltage (V_{DC})

iii) D.C power output (P_{DC}) iv) A.C input power (P_{AC})

Sol:

The average or DC value of a periodic waveform over one full cycle ($T = \frac{2\pi}{\omega}$) is calculated using integration.

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)$$

Since current flows only from 0 to π:

$$I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t)$$

$$I_{DC} = \frac{I_m}{2\pi}\left[-\cos(\omega t)\right]_0^{\pi}$$

$$I_{DC} = \frac{I_m}{2\pi}\left(-\cos(\pi) + \cos(0)\right)$$

$$I_{DC} = \frac{I_m}{2\pi}(1+1)$$

$$\mathbf{I_{DC} = \frac{I_m}{\pi}}$$

The average or DC voltage is simply the average current multiplied by the load resistance R_L:

$$V_{DC} = I_{DC} R_L$$

Substituting the expression for I_{DC}:

$$\mathbf{V_{DC} = \frac{I_m R_L}{\pi}}$$

Alternatively, using V_m as the peak output voltage (assuming ideal diode $r_f \ll R_L$), $V_{DC} = \frac{V_m}{\pi}$.

The DC power output is the power dissipated across the load resistance R_L due to the average DC current:

$$P_{DC} = I_{DC}^2 R_L$$

Substituting the expression for I_{DC}:

$$P_{DC} = \left(\frac{I_m}{\pi}\right)^2 R_L$$

$$\mathbf{P_{DC}} = \frac{\mathbf{I_m^2 R_L}}{\boldsymbol{\pi^2}}$$

The AC input power is the total power delivered by the source, which depends on the RMS value of the current (I_{rms}) flowing through the total circuit resistance ($R_L + r_f$).

First, we find the RMS current:

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2\, d(\omega t)}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2(\omega t)\, d(\omega t)}$$

$$I_{rms} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} \frac{1-\cos(2\omega t)}{2}\, d(\omega t)}$$

$$I_{rms} = \sqrt{\frac{I_m^2}{4\pi}\left[\omega t - \frac{\sin(2\omega t)}{2}\right]_0^{\pi}}$$

$$I_{rms} = \sqrt{\frac{I_m^2}{4\pi}((\pi - 0) - (0 - 0))}$$

$$I_{rms} = \sqrt{\frac{I_m^2 \pi}{4\pi}}$$

$$I_{rms} = \frac{I_m}{2}$$

Now, calculate the AC input power:

$$P_{AC} = I_{rms}^2 (R_L + r_f)$$

Substituting the expression for I_{rms}:

$$P_{AC} = \left(\frac{I_m}{2}\right)^2 (R_L + r_f)$$

$$P_{AC} = \frac{I_m^2 (R_L + r_f)}{4}$$

5.a) A 230V, 60Hz voltage is applied to the primary of a 5:1 step-down center-tapped transformer used in the full-wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together have a resistance of 100Ω, determine:
5M

i) DC voltage across the load
ii) DC current flowing to the load
iii) DC power delivered to the load
iv) PIV across each diode

Sol:

Step 1

The primary voltage (Vp) is 230 V and the turns ratio (n) is 5:1. The secondary voltage (Vs) can be calculated as Vs = Vp / n = 230 V / 5 = 46 V (RMS).

Step 2

For a full-wave rectifier, the DC voltage (Vdc) across the load is given by Vdc = (2 * Vs) / π. First, we convert Vs to peak voltage (Vp) using Vs_peak = Vs * √2 = 46 V * √2 ≈ 65 V. Thus, Vdc = (2 * 65 V) / π ≈ 41.2 V.

Step 3

The total resistance in the circuit is the load resistance (R_load = 900 Ω) plus the diode resistance (R_diode = 100 Ω), so R_total = 900 Ω + 100 Ω = 1000 Ω. The DC current (Idc) can be calculated using Ohm's law: Idc = Vdc / R_total = 41.2 V / 1000 Ω = 0.0412 A or 41.2 mA.

Step 4

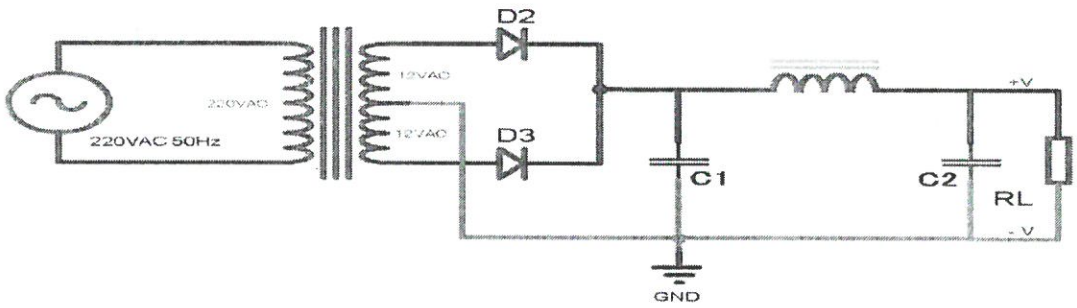
The Peak Inverse Voltage (PIV) for each diode in a full-wave rectifier is equal to the peak secondary voltage. Therefore, PIV = Vs_peak = 65 V.

Step 5

The DC power (Pdc) delivered to the load can be calculated using the formula Pdc = Vdc * Idc = 41.2 V * 0.0412 A ≈ 1.70 W.

b) Draw and explain the circuit diagram of full-wave rectifier with L-section filter. -5M

Sol: A full-wave rectifier with an L-section filter converts AC to DC using two diodes and a center-tapped transformer, with the filter consisting of an inductor (L) and a capacitor (C) placed in series with the load resistor (R_L). The rectifier stage produces pulsating DC, and the L-section filter smooths this by using the inductor to resist current changes and the capacitor to bypass remaining ripple, resulting in a smoother DC output.



Circuit diagram

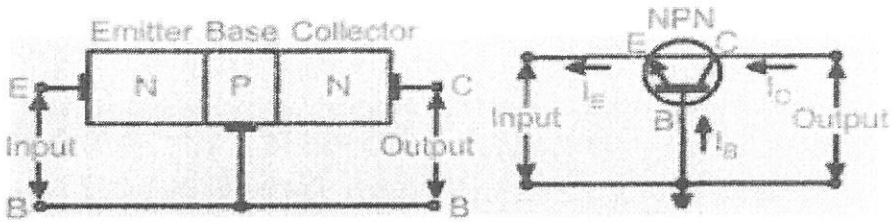
- **Input:** An AC source is connected to the primary winding of a center-tapped transformer.
- **Rectifier:** The secondary winding has a center tap and two ends. One end is connected to the anode of diode D_1 and the other to the anode of diode D_2. The cathode of both diodes is connected together.
- **Filter:** The L-section filter is formed by placing an inductor (L) in series with the load resistor (R_L) and a capacitor (C) in parallel across the load.
- **Output:** The final DC output is taken across the parallel combination of the inductor and the capacitor.

Explanation of operation

1. **Rectification:** During the positive half-cycle of the AC input, the top of the secondary winding is positive. Diode D_1 conducts, while D_2 is reverse-biased, and current flows through D_1 and the load.
2. **Rectification:** During the negative half-cycle, the bottom of the secondary winding becomes positive. Diode D_2 conducts, while D_1 is reverse-biased. Current flows through D_2 and the load. This makes the output current flow in the same direction in both half-cycles, producing a pulsating DC.
3. **Filtering (L-section):** The pulsating DC from the rectifier is fed to the L-section filter.
    1. **Inductor (L):** The inductor is placed in series with the load. An inductor opposes any change in current. When the current tries to drop, the inductor generates a back EMF that opposes the change, keeping the current flowing more steadily.
    2. **Capacitor (C):** The capacitor is placed in parallel with the load to act as a shunt filter. It charges up during the peaks and discharges during the valleys, smoothing out the remaining ripple that the inductor did not eliminate. The capacitor provides a low-impedance path for the AC ripple component to bypass the load, while blocking the DC component from passing through.

Unit III

6.a) With neat diagrams, explain the input and output characteristics of CB configurations.-5M
Sol:



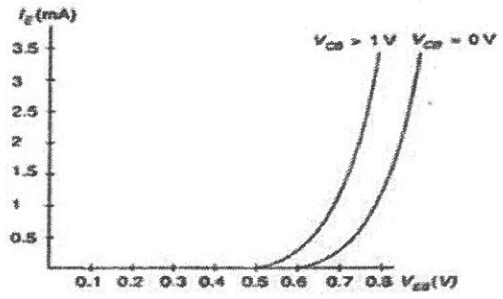
Common Base Configuration

Common base configuration:
Provides high current gain and moderate voltage gain. Suitable for impedance matching and RF amplifier circuits

In this type of connection:

- **Input** - Applied between **Emitter and Base**
- **Output** - Taken between **Collector and Base**
- The **Base** is common to both input and output → that's why it is called **Common Base (CB)**.

Input Characteristics (I_E vs V_{EB} at constant V_{CB})



CB input characteristics

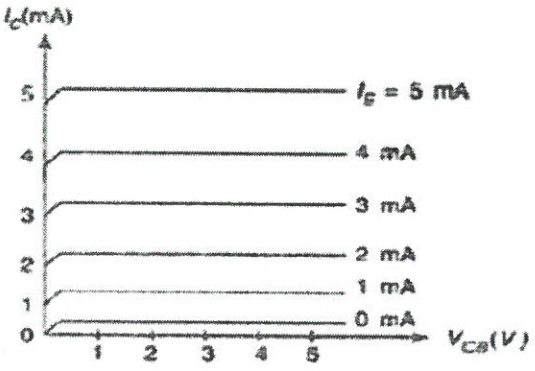
Input Voltage (V_{EB}): Voltage applied between **Emitter and Base**
Input Current (I_E): Current flowing into **Emitter**
Output Voltage (V_{CB}): Voltage between **Collector and Base**, kept constant

Graphical Representation:

The graph is drawn between **V_{EB} (x-axis)** and **I_E (y-axis)**

- When **V_{EB}** is small (less than ~0.5V), the emitter-base junction does not conduct much → **I_E is almost zero.**
- When **V_{EB}** crosses about **0.6–0.7 V** (for silicon transistor), the emitter-base junction conducts like a **diode**, so **I_E rises sharply.**
- If **V_{CB} increases**, the emitter-base junction gets a little more forward biased (due to collector pulling carriers), so **for the same V_{EB}, I_E is higher**. That's why the curve shifts left when V_{CB} > 1V.
- *It's like a friend giving you a push THAT you can start moving (current flows) sooner with less effort (lower VEB).*

Output Characteristics (I_C vs V_{CB} at constant I_E)



CB output characteristics

- **Output Voltage (V_{CB})**: Voltage applied between **Collector and Base** → x-axis
- **Output Current (I_C)**: Current flowing into **Collector** → y-axis
- **Input Current (I_E)**: Kept constant for each curve

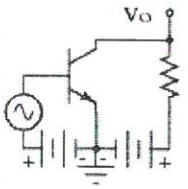
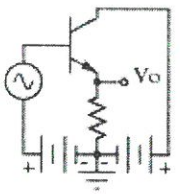
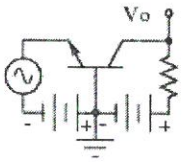
- **Graphical Representation:**
- For a fixed **I_E**, the **I_C remains almost constant** even when **V_{CB} increases.**
  - That's why the lines are almost horizontal.
  - Means: Collector current mainly depends on emitter current, not much on collector-base voltage.
- At very low **V_{CB} (close to 0)**, I_C is a little less because the collector is not pulling strongly yet.
- If you increase **I_E** (0 mA → 5 mA), the whole line shifts upward (bigger I_C).

Example:

- *Think of I_E as how much water you pour into a pipe.*
- *I_C is how much water comes out.*
- *V_{CB} is like the pipe's slope. A small slope change hardly affects flow; the water you pour (IE) is what really matters.*

b) Compare CB, CE and CC transistor configurations. **-5M**

Sol: **Any 5 comparisons**

Basic circuit	Common emitter	Common collector	Common base
			
Voltage gain	high	less than unity	high, same as CE
Current gain	high	high	less than unity
Power gain	high	moderate	moderate
Phase inversion	yes	no	no
Input impedance	moderate ≃ 1 k	highest ≃ 300 k	low ≃ 50 Ω
Output impedance	moderate ≃ 50 k	low ≃ 300 Ω	highest ≃ 1 Meg

(OR)

7.a) What is transistor biasing? Explain the need for biasing in transistor amplifiers. -5M

Sol: A **transistor** (BJT) is widely used as an amplifier and a switch.

- For a transistor to work properly as an amplifier, it must be operated in the **active region** of its characteristics.
  - This is achieved through a process called **biasing**.
- Biasing refers to applying suitable DC voltages and currents to the transistor terminals so that it operates in the desired region of its output characteristics
  - Without proper biasing, the transistor may not function correctly – it could go into cut-off, saturation, or give a distorted output.

Need for biasing

The necessity of transistor biasing arises due to the following reasons:

(i) To establish proper operating point
- *A transistor is biased to stay in the active region throughout the input cycle, preventing distortion from cutoff or saturation.*

(ii) To achieve faithful amplification
- *Output signal is an exact enlarged replica of the input signal without distortion*

(iii) To prevent thermal runaway
- *Without stabilization, IC can rise uncontrollably, causing thermal runaway and damaging the transistor.*

(iv) To minimize distortion
- *Proper biasing keeps the transistor in the linear region, so the signal is amplified without clipping or distortion.*

(v) To provide predictable performance
- *Biasing makes the circuit work reliably despite changes in transistor parameter β.*

b) Design a voltage divider bias network using a supply of 24V, β = 110 and I_{CQ} = 4mA, V_{CEQ} = 8V. Choose $V_E = V_{CC}/8$. -5M

Solution Given: $I_{CQ} = 4$ mA, $V_{CEQ} = 8$ V, $V_E = V_{CC}/8$, $V_{CC} = 24$ V, $\beta = 110$

(a) *To determine I_B, I_E and V_E:*

$$I_B = \frac{I_{CQ}}{\beta} = \frac{4 \times 10^3}{110} = 36.36\ \mu A$$

$$I_E = I_B + I_C = 36.36 \times 10^{-6} + 4 \times 10^{-3} = 4.03636\ mA$$

$$V_E = \frac{V_{CC}}{8} = \frac{24}{8} = 3\ V$$

(b) *To determine R_E and R_2:*

$$R_E = \frac{V_E}{I_E} = \frac{0.3}{4.03636 \times 10^{-3}} = 743.244\ \Omega$$

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

Therefore,

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{24 - 8 - 3}{4 \times 10^{-3}} = 3.25\ k\Omega$$

(c) *To determine R_1 and R_2*

$$V_B = V_E + V_{BE} = 3 + 0.7 = 3.7 \text{ V}$$

consider the current through R_1 be $I + I_B$ and that through R_2 be I. Resistors R_1 and R_2 forms the potential divider. For proper operation

of potential divider, current I should be atleast ten times the I_B. i.e. $I \geq 10\ I_B$. Therefore,

$$I = 10\ I_B = 10 \times 36.36 \times 10^{-6} = 363.6\ \mu\text{A}$$

$$R_2 = \frac{V_B}{I} = \frac{3.7}{363.6 \times 10^{-6}} = 10.176\ \text{k}\Omega$$

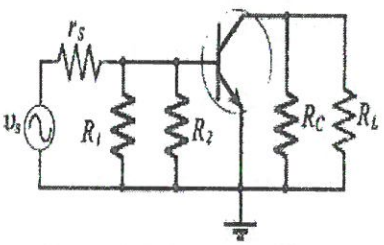
$$R_1 = \frac{V_{CC} - V_B}{I + I_B} = \frac{24 - 3.7}{(363.6 + 36.36) \times 10^{-6}} = 50.755\ \text{k}\Omega$$

Unit IV

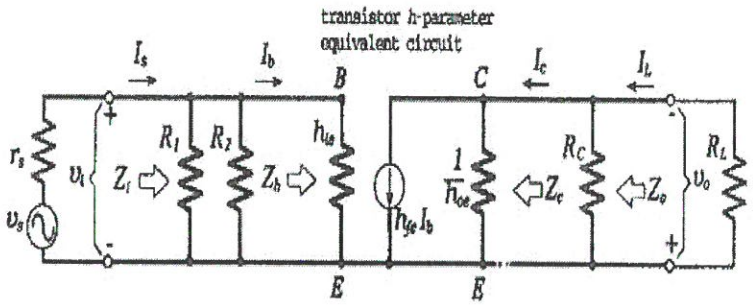
8.a) Analyze a single stage transistor amplifier using h-parameter. **-5M**

Sol:

Analyzing a single-stage transistor amplifier using h-parameters involves converting the transistor into its small-signal equivalent circuit and then applying the h-parameter model to find performance metrics like input impedance, output impedance, current gain, and voltage gain. The h-parameter model, a two-port network representation, uses four parameters (*hi,hr,hf,ho*) to describe the amplifier's behavior at low frequencies.



(a) *ac* equivalent circuit for *CE* transistor circuit



(b) *h*-parameter equivalent circuit for *CE* circuit

26
2
23

Apply h-parameter equations:

- Use the two main h-parameter equations for a two-port network:
  - $v_1 = h_{11}i_1 + h_{12}v_2 \Longrightarrow v_{in} = h_{ie}i_b + h_{re}v_{out}$
  - $i_2 = h_{21}i_1 + h_{22}v_2 \Longrightarrow i_c = h_{fe}i_b + h_{oe}v_{out}$

Calculate gain:

- **Current Gain (A_i):** The ratio of output current to input current. For a CE amplifier, the formula is approximately $A_i = \frac{-h_{fe}}{1 + h_{oe}R_L}$.
- **Voltage Gain (A_v):** The ratio of output voltage to input voltage. It can be calculated using the formula $A_v = -h_{fe}\frac{R_L}{h_{ie}}$.

Calculate impedance:

- **Input Impedance (Z_{in}):** The ratio of input voltage to input current. It can be expressed as $Z_{in} = \frac{v_{in}}{i_b}$. For a CE amplifier, this is given by

  $$Z_{in} = h_{ie} - \frac{h_{re}h_{fe}R_L}{1 + h_{oe}R_L}.$$

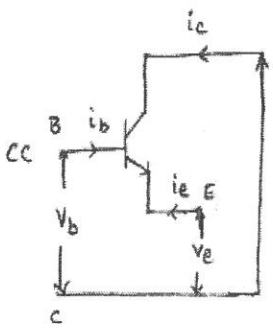
- **Output Admittance (Y_o):** The reciprocal of output impedance. It is given by

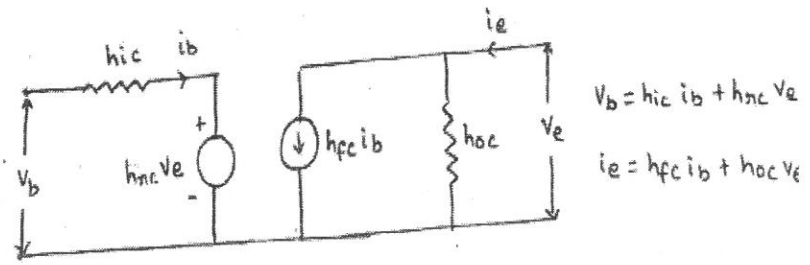
  $$Y_o = \frac{i_c}{v_c} = h_{oe} - \frac{h_{re}h_{fe}}{h_{ie} + R_s}.$$

- **Output Impedance (Z_o):** The reciprocal of the output admittance. $Z_o = \frac{1}{Y_o}$

b) Draw the circuit diagram of CC amplifier using hybrid parameter and derive the expressions for Ai, Av, Ri and Ro. **-5M**

Sol:





Current Gain (A_i)

The current gain A_i is defined as the ratio of output current to input current, $A_i = I_e/I_b$, or using our two port definition $A_i = I_2/I_1$. Using the **h-parameter** equations for the CC configuration:

$$V_1 = h_{ic}I_1 + h_{rc}V_2$$

$$I_2 = h_{fc}I_1 + h_{oc}V_2$$

With a load resistor R_L, the output voltage is $V_2 = -I_2R_L$. Substituting V_2 into the second equation:

$$I_2 = h_{fc}I_1 + h_{oc}(-I_2R_L)$$

$$I_2(1 + h_{oc}R_L) = h_{fc}I_1$$

$$A_i = \frac{I_2}{I_1} = \frac{h_{fc}}{1 + h_{oc}R_L}$$

Input Resistance (R_i)

The input resistance R_i is defined as the ratio of input voltage to input current, $R_i = V_1/I_1$, with the load connected. Using the V_1 equation and substituting $V_2 = -I_2R_L = -A_iI_1R_L$

$$V_1 = h_{ic}I_1 + h_{rc}(-A_iI_1R_L)$$

$$R_i = \frac{V_1}{I_1} = h_{ic} - h_{rc}A_iR_L$$

Substituting the expression for A_i:

$$R_i = h_{ic} - \frac{h_{rc}h_{fc}R_L}{1 + h_{oc}R_L}$$

Voltage Gain (A_v)

The voltage gain A_v is the ratio of output voltage to input voltage, $A_v = V_2/V_1$.

$$A_v = \frac{-I_2R_L}{V_1} = \frac{-A_iI_1R_L}{R_iI_1} = \frac{-A_iR_L}{R_i}$$

Substituting the expressions for A_i and R_i and simplifying yields:

$$A_v = \frac{-h_{fc}R_L}{h_{ic} + (h_{ic}h_{oc} - h_{rc}h_{fc})R_L}$$

Output Resistance (R_o)

The output resistance R_o is the resistance seen looking into the output terminals with the input source resistance R_S connected and the source voltage set to zero ($V_S = 0$). This implies $V_1 = -I_1 R_S$.

Substituting V_1 into the first ***h*-parameter** equation:

$$-I_1 R_S = h_{ic} I_1 + h_{rc} V_2 \Longrightarrow I_1 = \frac{-h_{rc} V_2}{h_{ic} + R_S}$$

Substituting this I_1 into the second ***h*-parameter** equation:

$$I_2 = h_{fc}\left(\frac{-h_{rc} V_2}{h_{ic} + R_S}\right) + h_{oc} V_2$$

$$I_2 = V_2\left[h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_S}\right] = V_2\left[\frac{h_{oc}(h_{ic} + R_S) - h_{fc} h_{rc}}{h_{ic} + R_S}\right]$$

The output resistance is $R_o = V_2/I_2$ (assuming test current $I_x = I_2$ flows into the network):

$$R_o = \frac{h_{ic} + R_S}{(h_{ic} h_{oc} - h_{fc} h_{rc}) + h_{oc} R_S}$$

9.a) Derive the expressions for Ai, Av, Ri and Ro of CB amplifier using approximate model.7M
Sol:

ANALYSIS OF CB AMPLIFIER USING THE APPROXIMATE MODEL

Figure 6.13 shows the equivalent circuit of CB amplifier using the approximate model, with the base grounded, input signal applied between emitter and base and load connected between collector and base.

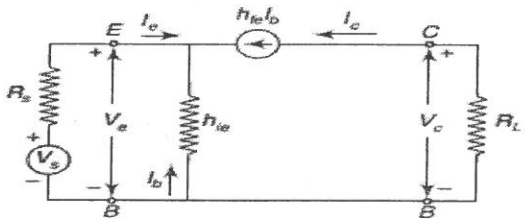


Fig. 6.13 *Simplified hybrid model for the CB circuit*

Current gain

$$A_I = \frac{-I_c}{I_e} = \frac{-h_{fe} I_b}{I_e} = \frac{-h_{fe} I_b}{-(h_{fe} I_b + I_b)} = \frac{h_{fe}}{1 + h_{fe}} = -h_{fb}, \text{ from Table 6.3}$$

Hence, current gain, $A_I = \dfrac{h_{fe}}{1 + h_{fe}} = -h_{fb}$

Input resistance $R_i = \dfrac{V_e}{I_e} = \dfrac{-I_b h_{ie}}{-(1 + h_{fe}) I_b} = \dfrac{h_{ie}}{1 + h_{fe}} = h_{ib}$

Voltage gain $A_V = \frac{V_c}{V_e} = \frac{-h_{fe} I_b R_L}{-I_b h_{ie}} = \frac{h_{fe} R_L}{h_{ie}}$

A_i, A_V and R_i do not differ from exact values by more than 10%.

Output impedance $R_o = \frac{V_c}{I_c}$ with $V_s = 0$, $R_L = \infty$

With $V_s = 0$, $I_e = 0$ and $I_b = 0$

Hence, $I_c = 0$.

Therefore, $R_o = \infty$ using the approximate model.

b) The h-parameters of a transistor used in a common emitter circuit are hie = 1 kΩ, hre = 10 × 10^{-4}, hfe = 50, hoe = 25 × 10^{-6}. The load resistance for the transistor is 1 kΩ in the collector circuit. Determine Ai, Av, Ri and Ro in the amplifier stage (Assume Rs = 1000 Ω) -5M

Sol:

Step 1: Calculate Current Gain (A_i)

The formula for the current gain (A_i) of a CE amplifier stage is given by:

$$A_i = \frac{h_{fe}}{1 + h_{oe} R_L}$$

Substituting the given values:

$$A_i = \frac{50}{1 + (25 \times 10^{-6}\ \text{S}) \times (1000\ \Omega)}$$

$$A_i = \frac{50}{1 + 0.025} = \frac{50}{1.025}$$

$$A_i \approx 48.78$$

Step 2: Calculate Input Resistance (R_i)

The formula for the input resistance (R_i) of the amplifier stage is given by:

$$R_i = h_{ie} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L}$$

Substituting the values:

$$R_i = 1000\ \Omega - \frac{(0.001) \times (50) \times (1000\ \Omega)}{1 + (25 \times 10^{-6}\ \text{S}) \times (1000\ \Omega)}$$

$$R_i = 1000\ \Omega - \frac{50}{1.025}$$

$$R_i = 1000\ \Omega - 48.78\ \Omega$$

$$R_i \approx \mathbf{990.2\ \Omega}$$

Step 3: Calculate Voltage Gain (A_v)

The formula for the voltage gain (A_v) of the amplifier stage is given by:

$$A_v = -\frac{A_i R_L}{R_i}$$

Substituting the calculated values:

$$A_v = -\frac{48.78 \times 1000\ \Omega}{990.2\ \Omega}$$

$$A_v = -\frac{48780}{990.2}$$

$$A_v \approx \mathbf{-48.2}$$

Step 4: Calculate Output Resistance (R_0)

The formula for the output resistance (R_o) considering the source resistance (R_s) is:

$$R_o = \frac{R_s + h_{ie}}{h_{oe}(R_s + h_{ie}) - h_{re}h_{fe}}$$

Substituting the values:

$$R_o = \frac{1000\ \Omega + 1000\ \Omega}{25 \times 10^{-6}\ \text{S} \times (1000\ \Omega + 1000\ \Omega) - 0.001 \times 50}$$

$$R_o = \frac{2000\ \Omega}{25 \times 10^{-6}\ \text{S} \times 2000\ \Omega - 0.05}$$

$$R_o = \frac{2000\ \Omega}{0.05 - 0.05}$$

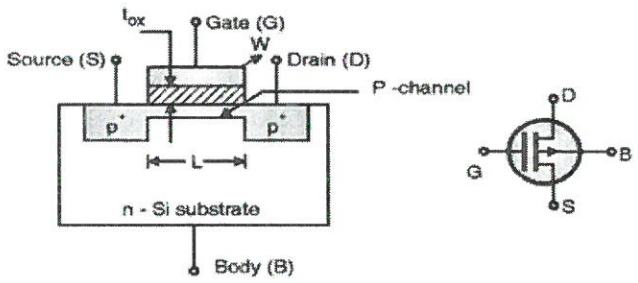
$$R_o = \frac{2000\ \Omega}{0} \approx \infty$$

Unit V

10.a) Explain the constructional features of a depletion mode P-channel and explain its basic operation. **-5M**

Sol: **Depletion Mode MOSFET**

- **Default State :** The device is normally **ON**.
- **Channel Conductivity:**
  - Conductivity is at its **maximum** when no gate voltage is applied.
- **Effect of Gate Voltage:**
  - Applying a gate voltage (either **positive or negative**) **decreases** the channel conductivity.
- **Function:**
  - The gate voltage is used to *deplete* (reduce) the existing channel and turn the device OFF.



(a) Cross-sectional view **(b) Symbol**

p-channel depletion mode MOSFET

Channel at Zero Gate Voltage (VGS = 0)

- A **P-type channel already exists** between source and drain.
- Since it is a *depletion-mode* device, this channel is present by default.
- So current flows from **Source → Drain** when a voltage **VSD** is applied.

✔ The device behaves as **normally ON**.

Applying a Negative Gate Voltage (VGS < 0) — Enhances Conduction

- A **more negative gate** attracts holes (majority carriers) into the channel.
- This **increases** the channel's hole concentration.
- Channel becomes **more conductive → more current flows**.

✔ Negative gate voltage **enhances conduction**.

Applying a Positive Gate Voltage (VGS > 0) — Depletes the Channel

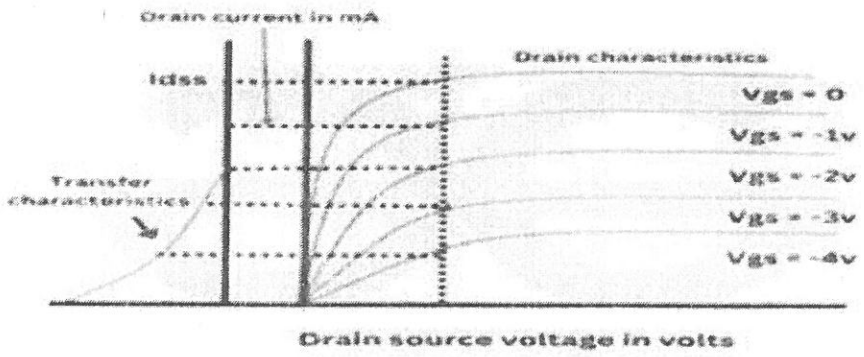
- A **positive gate** repels holes from the channel.
- This reduces the number of carriers → channel becomes weaker.
- At sufficiently positive VGS, the channel is pushed towards cutoff.

✔ Positive gate voltage **reduces conduction** (depletion).
✔ If gate voltage is high enough, the MOSFET turns **OFF**.

b) Explain the drain characteristics and transfer characteristics of a JFET. **-5M**

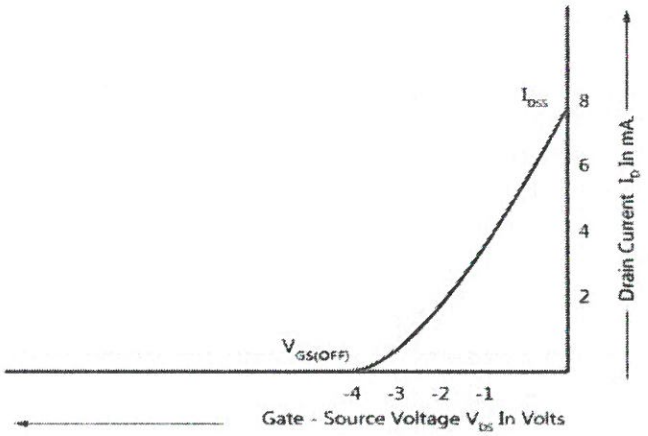
Sol: Drain characteristics show the relation between **Drain Current (ID)** and **Drain-to-Source Voltage (VDS)** at different **Gate-to-Source Voltage (VGS)** values.

ID vs. VDS for different VGS values.



A JFET operates in three regions:
Ohmic (Linear) Region
Saturation or Active Region
Cutoff Region

TRANSFER CHARACTERISTICS of a JFET
Transfer characteristics show the relation between:
Drain current (ID) and **Gate-to-Source voltage (VGS) at a constant VDS (in saturation region).**



Transfer Characteristics of JFET

Shape of the curve

- It is a **parabolic** relationship.
- It follows the **Shockley's equation**:

Key Points

(a) At VGS = 0

- Drain current is maximum:

(b) As VGS becomes more negative

- I_D decreases following a parabolic curve.

(c) At VGS = VGS(off)

- Drain current becomes **zero**:

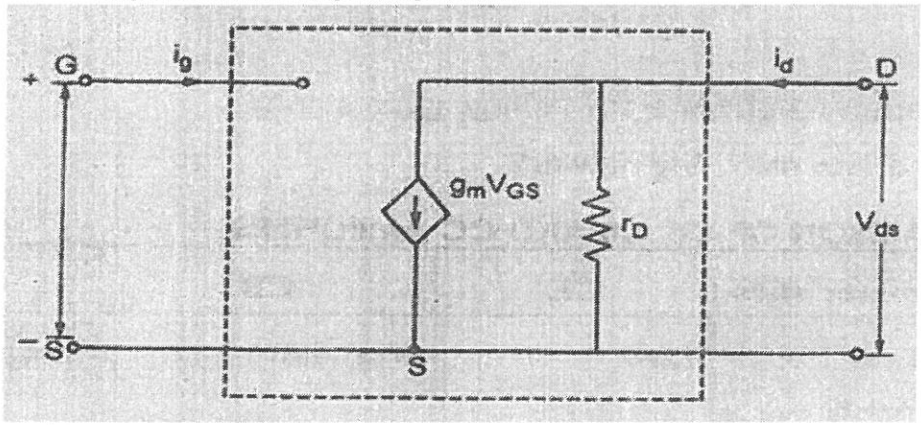
✔ JFET is OFF.
✔ Channel completely pinched off.

11 a) Summarize Small Signal Model of JFET. **-5M**

Sol:

Introduction

- The **small-signal model** shows how a FET works when a **small AC signal** is applied along with the **DC bias**.
- This model helps in **analyzing amplifier circuits**, such as determining **voltage gain, input impedance**, and **output impedance**.



Parameters Used in Small-Signal Model:

1. **Transconductance (gm):**
   - It is the ratio of change in drain current to the corresponding change in gate-source voltage, keeping V_{DS} constant.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$$

   - Units: Siemens (S)
2. **Drain Resistance (rd):**
   - It represents the **output resistance** of the FET due to the channel.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$$

3. **Gate Resistance (RG):**
   - The gate is reverse biased, so the input current is nearly zero.

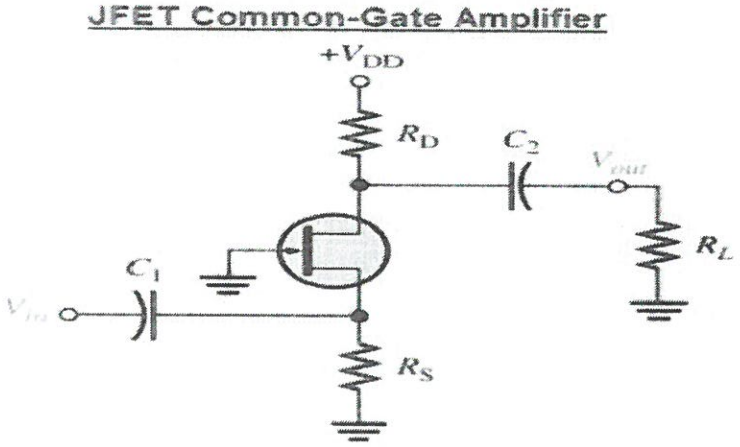
$$R_{in} \approx \infty$$

b) With neat diagrams, explain the circuit and small-signal analysis of a Common Gate (CG) amplifier. **-5M**

Sol: A Common-Gate MOSFET amplifier is one where the gate terminal is AC-grounded, the input is applied at the source, and the output is taken at the drain.

It is mainly used for:

- **High-frequency applications**
- **Low input impedance circuits**
- **Current buffering**

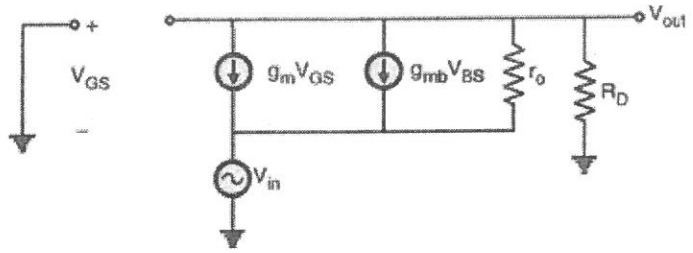


BASIC OPERATION

- The **signal enters through the source**, making the transistor modulate current based on the small variations in **vgs**.
- Since the **gate is at AC ground**,

$$V_{gs}=-V_{in}$$

- **Drain current i_d changes** with the input signal.
- Changing drain current causes a voltage drop in RD, producing the output voltage.



small signal equivalent circuit of the CG amplifier

Voltage Gain A_v

From the small-signal model:

- Gate is at AC ground →

$$v_{gs} = -v_{in}$$

Drain current:

$$i_d = g_m v_{gs} = -g_m v_{in}$$

Output voltage at drain:

$$v_{out} = -i_d R_D = g_m v_{in} R_D$$

Thus the **voltage gain** is:

$$\boxed{A_v = g_m R_D}$$

Input Resistance R_{in}

Input seen at the source:

$$R_{in} \approx \frac{1}{g_m}$$

Output Resistance

$$R_{out} \approx r_o \parallel R_D$$

Current Gain

Approximately unity:

$$A_i \approx 1$$

Because the CG amplifier behaves like a **current buffer.**