4/4 B.Tech - EIGHTH SEMESTER

EC 8T3A **Digital System Design through Verilog** **Credits: 4**

Lecture : 4 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks**

Course objectives:

- To study the basic elements of Verilog HDL.
- To understand the various modelling used to represent hardware in Verilog HDL.
- To learn about the state machine implementation using Verilog HDL.
- To study the programming with programmable gate arrays and CPLDs.

Learning Outcomes:

- Explain the structure and fundamental components of digital systems
- Describe the fundamental architecture of digital functional units such as data converters, ALUs, and memory
- Analyze and synthesize design interfaces between two or more digitalmodules, using various handshaking and responsive pair protocols
- Use the Verilog design, synthesize, test and modeling tools

UNIT-I

Introduction To Verilog: Verilog as HDL, Levels of design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

Language Constructs And Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT-II

Gate Level Modeling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip – Flops with gate primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

UNIT-III

Behavioral Modeling: Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait Construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-Blocking Assignments, The case statement, Simulation Flow if and if-else constructs, assign – deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT-IV

Modeling at Data Flow Level: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators. **Switch Level Modeling**: Introduction, Basic Transistor Switches, CMOS Switch, Bi – directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

UNIT-V

System Tasks, Functions, And Compiler Directives: Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File – Based Tasks and Functions, Compiler Directives, Hierarchical Directives, Hierarchical Access, General Observations, Exercises.

Functions, Tasks And User – Defined Primitives: Introduction, Function, Tasks, User-defined Primitives (UDP), FSM Design (Moore and Melay Machines).

UNIT-VI

Digital Design With SM Charts: State Machine Charts, Derivation of SM Charts, Realization of SM Charts, Implementation of the Dice Game, Alternative realizations for SM Charts using Microprogramming Linked State Machines.

UNIT-VII

Designing With Programmable Gate Arrays And Complex Programmable Logic Deivices: Xilinx 3000 Series FPGA's, Designing with FPGAs, using a One – Hot state Assignment, Altera Complex programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

UNIT-VIII

Verilog Models: Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design, Design of Microcontroller CPU.

Learning Resources

Text Books:

1. Design through Verilog HDL – T. R. Padmanabhan and B. Bala Tripura Sundari, WSE, IEEE Press, 2004.
2. A Verilog Primier – J. Bhaskar, BSP, 2003.

References:

1. Fundamentals of Logic design with Verilog – Stephen Brown and Zvonko Vranesic, TMH, 2007
2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.
3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.
4. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.