Advanced Digital Design

Course Code	20EC4701B	**Year**	IV	**Semester**	I
Course Category	PE-III	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Logic Gates, Boolean Algebra & K-Maps
Continuous Internal Evaluation	30	**Semester End Evaluation**	70	**Total Marks**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Perform Binary arithmetic operations using Complements & Work effectively with IEEE FP numbers (L3).
CO2	Design Combinational circuits upto subsystem level preferably using functional blocks and gates wherever necessary based on the specifications (L5).
CO3	Analyze the timing behavior, delays, and hazards in combinational circuits and fix hazards due to single-bit time-varying binary signals (L4).
CO4	Design and Analyze Sequential circuits using a state machine design approach upto the introductory subsystem level based on the specifications (L5).
CO5	Fix set-up and hold violations of Sequential circuits (L4).

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3													
CO2			3						3				2	
CO3		2							3				2	
CO4		3	3						3				2	
CO5			2						2				1	
Average* (Rounded to nearest integer)	**3**	**3**	**3**						**3**				**2**	

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**PROCESSOR ARITHMETIC:** Numbers with different bases, Two's complement number system - Arithmetic operations. Fixed-point number system, Floating-point number system - IEEE 754 format.	CO1
II	**COMBINATIONAL CIRCUITS**: CMOS logic design, Combinational circuits, Timing hazards, Basic functional blocks - Decoders, Encoders, Multiplexers,	CO2, CO3

	Parity Circuits, Comparators, Adders, Subtractors. Carry-look-ahead adder – timing analysis.	
III	**SEQUENTIAL LOGIC**: Latches and flip-flops, Sequential logic circuits - timing analysis (set-up and hold times). State machines - Mealy & Moore machines, FSM design using D Flip-Flops, Synchronizers and meta-stability and basics of clock domain crossing. FSM applications-Vending Machine, Traffic light controller.	CO3, CO4
IV	**SUBSYSTEM DESIGN USING FUNCTIONAL BLOCKS - I**: Larger combinational designs involving basic combinational functional blocks - ALU, 4-bit combinational Multiplier, Barrel shifter, Dual Priority Encoder and Cascading Comparators.	CO2
V	**SUBSYSTEM DESIGN USING FUNCTIONAL BLOCKS - II**: Design of larger logical blocks involving sequential/combinational functional blocks - Pattern (sequence) generator/detector(s), Programmable up-down counters, Programmable FIFO controllers.	CO2, CO4

Learning Resources
Text Books
1. John F. Wakerly, "Digital Design", 3rd Ed., PH, 2002 & 4th Ed., PH, 2006.
Reference Books
1. Randy H. Katz and Gaetanao Boriello , "Contemporary Logic Design" 2nd Ed., PH, 2005. 2. Charles Roth, Jr., Larry Kinney, Fundamentals of Logic Design, 7/e, Cengage Learning, India, 2013.
e- Resources & other digital material
1. http://www.ece.ubc.ca/~saifz/eece256.html 2. http://nptel.iitm.ac.in/courses/Webcourse-contents/IIT%20Guwahati/digital_circuit /frame/index.html