Advanced Physical Design

Course Code	20EC2701D	**Year**	IV	**Semester**	I
Course Category	Open Elective-III	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Nil
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Design power-mesh for the given specifications, and analyze IR drop and EM issues.(L3)
CO2	Implement the low power intent of the design using industry standard UPF(L3)
CO3	Verify whether the design meets the power intent in UPF (L3)
CO4	Analyze and fix chip-timing issues by considering on-chip variations(L4)
CO5	Perform physical verification both at LVS & DRC level and fix all issues(L3)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	3	3	2	2	3								3	1
CO2	2	3	2	2	3								3	1
CO3	3	2	2	2	3								3	1
CO4	3	2	2	2	3								3	1
CO5	3	2	2	2	3								3	1
Average * (Rounded to nearest integer)	**3**	**2**	**2**	**2**	**3**								**3**	**1**

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**Power Analysis** Introduction to power analysis, Goals and objectives, Data preparation, Power mesh design, Static IR analysis, Dynamic IR analysis, Signal and power EM. Types of Power consumption in CMOS Circuits.	CO1
II	**Low Power Design** - I Introduction, Low Power optimization in the SOC flow, Architectural techniques for low power, Special cells for power management, Gate level Low Power Techniques	CO2
III	**Low Power Design** - II	CO3

	Low Power Implementation Techniques (Multi-Voltage, Power Gating, etc.), UPF formats, Low Power checks.	
IV	**Advanced STA** Hierarchical STA (ILM, XILM, ETM), On-chip Variations(OCV), Advanced On-Chip Variations(AOCV), Parametric On-Chip Variations(POCV), Introduction to LVF.	CO4
V	**Physical Verification**: Physical verification - Introduction, goals and objectives, Design Rule Check(DRC), Layout Versus Schematic check(LVS), and Electrical Rule Check(ERC). Design for Manufacturability (DFM): Introduction, DFM aware routing, DFM checks and fixing (Pattern Matching, MAS).	CO5

Learning Resources
Text Books
1. Rakesh Chadha and J. Bhasker, "An ASIC Low Power Primer", Springer, 2013 2. Voltus Reference Manuals, 17.12.000 3. Tempus Reference Manual, 17.12.000
Reference Books
1.Calibre Reference Manual, 2017.1_17.12
