COMPUTER ORGANIZATION AND ARCHITECTURE

Course Code	20EE4501E	**Year**	III	**Semester(s)**	I
Course Category	Professional Elective-I	**Branch**	EEE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	-
Continuous Internal Evaluation:	**30**	**Semester End Evaluation:**	**70**	**Total Marks:**	**100**

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Understand the basic functional units of a computer system and its organization. (L2)
CO2	Apply appropriate instructions for processing various types of computers operations. (L3)
CO3	Apply various types of organizations on registers. (L3)
CO4	Analyze memory hierarchy, I/O communication and pipelining. (L4)

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3:High, 2: Medium, 1:Low)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3													3
CO2	2								1	1			2	2
CO3	2								1	1			2	2
CO4		2							1	1			2	

SYLLABUS		
Unit No.	**Contents**	**Mapped CO**
I	**Register Transfer and Micro-Operations:** Register Transfer Language, Register Transfer, memory Transfers, Bus construction with Multiplexers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift Unit.	**CO1, CO2**
II	**Basic Computer Organization:** Instruction codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input- Output and Interrupt.	**CO1, CO2**
III	**Central Processing Unit:** General registers Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transferand Manipulation, Program Control.	**CO1, CO3**
IV	**Computer Arithmetic:** Introduction, Addition and Subtraction, Booth Multiplication Algorithm. **Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary memory, Associative Memory, Cache Memory, Virtual Memory.	**CO1, CO2, CO4**

V	**Input-Output Organization:** Peripheral Devices, Input-output Interface, Asynchronous Data Transfer, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor. **Pipeline and Parallel Processing:** Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline.	**CO1, CO4**

Learning Resources
Text Books
1. Morris M. Mano, Computer System Architecture, Pearson., Third Edition, 1992,
Reference Books
1. William Stallings, Computer Organization and Architecture, PHI, Eighth Edition, 2010. 2. Carl Hamachar, Vranesic, Computer Organization, McGraw Hill, 2002.
Web Links 1. https://nptel.ac.in/courses/106/106/106106092/