DIGITAL DESIGN USING VERILOG HDL

Course Code	20EC5501	**Year**	III	**Semester**	I
Course Category	MINOR	**Branch**	ECE	**Course Type**	Theory
Credits	4	**L-T-P**	3-1-0	**Prerequisites**	Digital Logic Design
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Understand the language constructs and programming fundamentals of Verilog HDL. (L2)
CO2	Choose the suitable abstraction level for a particular digital design (L3).
CO3	Construct Combinational and sequential circuits in different modelling styles using Verilog HDL (L3).
CO4	Analyse and Verify the functionality of digital circuits/systems using test benches (L4).

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	2									2				
CO2	2									2				
CO3	2								2	2		2		2
CO4		3							2	2		2		2
Average* (Rounded to nearest integer)	2	3							2	2		2		2

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**Introduction to Verilog HDL:** Verilog as HDL, Levels of Design Description, Concurrency, Program structure, Top-down and Bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block, Verilog Data types and Operators, system tasks, compiler directives.0	CO1, CO2
II	**Gate-Level Modelling:** Modelling using basic Verilog gate Primitives,	CO1,

	Description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays, Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in Gate-level Modelling.	CO3
III	**Dataflow Modelling:** Continuous assignments, Delay specification, expressions, operators, Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in dataflow model.	CO1, CO3
IV	**Behavioral Modelling: Procedural Assignments,** Initial and always blocks, blocking and non-blocking statements, delay control, conditional statements, Multiway branching, loops, sequential and parallel blocks, Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in Behavioral model.	CO1, CO3
V	**Components Test and Verification:** Test Bench - Combinational Circuits Testing, Sequential Circuits Testing, Test Bench Techniques, Design Verification, Assertion Verification.	CO1, CO4

Learning Resources
Text Books
1. Samir Palnitkar-Verilog HDL: A Guide to Digital Design and Synthesis, Pearson Education, 2nd Ed., 2009. 2. Michel D. Ciletti- Advanced Digital Design with Verilog HDL,2nd Ed., PHI, 2009
Reference Books
1 Padmanabhan, Tripura Sundari -Design through Verilog HDL, Wiley, 2016 2. S.Brown, Zvonko – Vranesic, Fundamentals of Digital Logic with Verilog Design, TMH, 3rd Ed., 2014.
e- Resources
1. http://www.ece.ubc.ca/~saifz/eece256.html 2. http://nptel.iitm.ac.in/courses/Webcourse-contents/IIT%20Guwahati/digital_circuit /frame/index.html

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