Course Code	20EC4501D	Year	III	Semester	Ι	
Course Category	PE-I	Branch	ECE	Course Type	Theory	
Credits	3	L-T-P	3-0-0	Prerequisites	-	
Continuous Internal Evaluation	30	Semester End Evaluation	70	Total Marks	100	

### COMPUTER ARCHITECTURE AND ORGANIZATION

## **Course Outcomes**

After successful completion of the course, the student will be able to

**CO1** Understand the basic functional units of a computer system and its organization. L2

**CO2** Apply appropriate instructions for processing various types of computer operations. L3

**CO3** Apply various types of organizations on registers L3

CO4 Analyze memory hierarchy, I/O communication and pipelining. L4

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3-High 2: Madium 1:Law)														
$C_{0}$ D01 D02 D03 D04 D05 D04 D07 D08 D00 D0 D0 D0 D0 D0														
COS	FUI	FU2	105	FU4	105	FUU	FU/	100	109	10	11	12	1	2
CO1	3					2	2							
CO2	2					2	2			1			2	1
CO3	2					2	2			1			2	1
<b>CO4</b>		2				2	2			1			2	1

Syllabus					
UNIT NO.	Contents	Mapped COs			
Ι	Register Transfer and Micro-Operations: Register Transfer Language, Register Transfer, memory Transfers, Bus construction with Multiplexers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift Unit.	CO1,CO2			
Π	Basic Computer Organization: Instruction codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory Reference Instructions, Input- Output and Interrupt.	CO1,CO2			
III	Central Processing Unit: General registers Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control	CO1,CO3			
IV	Computer Arithmetic: Introduction, Addition and Subtraction, Booth Multiplication Algorithm. Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associative Memory, Cache Memory, Virtual Memory.	CO1,CO2 CO4			
V	Input-Output Organization: Peripheral Devices, Input-output Interface, Asynchronous Data Transfer, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor. Pipeline and Parallel Processing: Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline	CO1,CO4			

### **Learning Resources**

### **Text Books**

Morris M. Mano - Computer System Architecture, 3<sup>rd</sup> Ed., 1992, Pearson.
William Stallings - Computer Organization and Architecture, 8<sup>th</sup> Ed., 2010, PHI.

# **Reference Books**

1. Carl Hamachar, Vranesic - Computer Organization, 2002, McGraw Hill.

e- Resources and other Digital Material

1. https://nptel.ac.in/courses/106/106/106106092/