DIGITAL INTEGRATED CIRCUITS AND APPLICATIONS

Course Code	20EC4501B	**Year**	III	**Semester**	I
Course Category	Professional Elective	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	DLD
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	**Understand** the basic features of Verilog HDL and logic families(L2)
CO2	**Build** different levels of Modelling in Verilog HDL and logic gates using different logic families (L3)
CO3	**Develop** Verilog HDL code for various digital ICs of combinational logic (L3)
CO4	**Develop** Verilog HDL code for various digital ICs of sequential logic (L3)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)
Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation
*** - Average value indicates course correlation strength with mapped PO**

COs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO10**	**PO11**	**PO 12**	**PSO 1**	**PSO 2**
CO1		2			2								2	
CO2	3				3								3	
CO3	2				2								2	
CO4	2				2								2	
Average* (Rounded to nearest integer)	**2**	**2**			**2**								**2**	

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**Introduction to Verilog** Need for HDL, Historical development of Verilog, Module: Design module, Test bench, Importance of Verilog in VLSI, Verilog data types and operators	CO-1, CO-2
II	**Different levels of Modelling** Gate level modelling: Gate types, Gate delays. Data flow modelling: Continuous assignments, delays. Behavioral Modelling :initial statement, always statement, procedural assignments, conditional statements, multi way branching, loops	CO-1, CO-2
III	**Logic Families** Introduction to logic families, CMOS logic, TTL families, CMOS/TTL interfacing, low voltage CMOS logic and interfacing, Comparison of logic families, Familiarity with standard 74XX series-ICs and 40 XX series-ICs.	CO-1, CO-2
IV	**Verilog models of the Combinational Logic ICs.** Decoders, encoders, three state devices, multiplexers and demultiplexers, Code Converters, comparators, adders & subtractors, ALUs, Combinational multipliers	CO-1,CO-2, CO-3

V	**Verilog models of the Sequential Logic ICs.** Latches, flip-flops, counters and shift registers, impediments to synchronous design.	CO-1,CO-2, CO-4

Learning Resources
Text Books
1. Samir Palnitkar - Verilog HDL – A Guide to Digital Design and Synthesis, 2nd Ed., Pearson Publishers, 2003 2. John F. Wakerly - Digital Design Principles & Practices – PHI/ Pearson Education Asia, 3rd Ed.,2005
Reference Books
1. J. Bhasker - Verilog Primer –, Pearson Education/ PHI, 3rd Ed.,2003 2. Alan B. Marcovitz - Introduction to Logic Design –TMH, 2nd Ed.,2003
E Resources:
1. https://www.youtube.com/watch?v=FWE0-FOoE4s&list=PLUtfVcb-iqn-EkuBs3arreilxa2UKIChl 2. https://www.youtube.com/watch?v=ow_gCaxPnmc

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