Code No: R05220403 **Set No. 1**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2007
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Perform the following using BCD arithmetic. Verify the result. [2 X 4 = 8]
   i. $1273_{10} + 9587_{10}$
   ii. $7762_{10} + 3838_{10}$
   (b) Convert the following. [4 X 2 = 8]
   i. $977_{10} = (\quad)_{16}$
   ii. $657_{10} = (\quad)_{8}$
   iii. $754_{10} = (\quad)_{2}$
   iv. $1001_{16} = (\quad)_{10}$

2. (a) Reduce the following Boolean expressions. [8]
   i. (AB' + AC')(BC + BC')(ABC)
   ii. AB'C + A'BC + ABC
   iii. (ABC)'(A + B + C)'
   iv. A + B'C (A + (B'C)')
   (b) Obtain the Dual of the following Boolean expressions. [8]
   i. ABC + A'B + ABC'
   ii. (BC' + A'D)(AB' + CD')
   iii. x'yz + xz
   iv. xy + x (wz + wz')

3. Apply Branching method to simplify the following function
   F (A, B, C, D) = $\prod M(0, 1, 4, 5, 9, 11, 13, 15, 16, 17, 25, 27, 28, 29, 31)d(20, 21, 22, 30)$. [16]

4. (a) Design a circuit to convert Excess-3 code to BCD code Using discrete Logic gates.
   (b) Design a 3 to 8 decode using 2 to 4 decodes and other required gates. [8+8]

5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

(b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Design a sequence detector which detects 110010 Implement the sequence detector by using D - type flipflops

   (b) Classify the required circuits into synchronous, asynclironus, clockmode, pulse mode with suitable examples. [8+8]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.

   (a) Obtain State - Diagram.

   (b) Also obtain state - Table.

   (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, other wise go to T_3.

   (b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

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Code No: R05220403 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows? [4 × 4 = 16]
   (a) 001111101010
   (b) 101110010110
   (c) 101110110100
   (d) 110011010111

2. (a) Reduce the following Boolean expressions. [8]
      i. ((AB)' + A' + AB)'
      ii. AB + (AC)' + AB' + C(AB + C)
      iii. ((AB' + ABC)'+ A(B + AB'))'
      iv. AB + A(B + C) + B(B + C)
   (b) Obtain the Dual of the following Boolean expressions. [8]
      i. x'y' + xy + x'y
      ii. xy' + y'z' + x'z'
      iii. x' + xy + xz' + xy'z'
      iv. (x + y)(x + y')

3. (a) What are the advantages and disadvantages of the tabular method vis--vis the K-map? [6]
   (b) Reduce the following function using K-map
   F = $\prod M(1, 4, 5, 6, 7, 8, 9, 14, 15, 22, 23, 24, 25, 28, 29, 30, 31)$ [10]

4. (a) What is an Encoder? What are the advantages of priory Encoder over Encoder.
   (b) Design and implement a two bit comparator using logic gates. [6+10]

5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

(b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Compare synchronous & Asynchronous circuits

   (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

7. Clocked sequential circuit with two inputs and and a single output Z using J - K flip flops is as shown in figure 7:

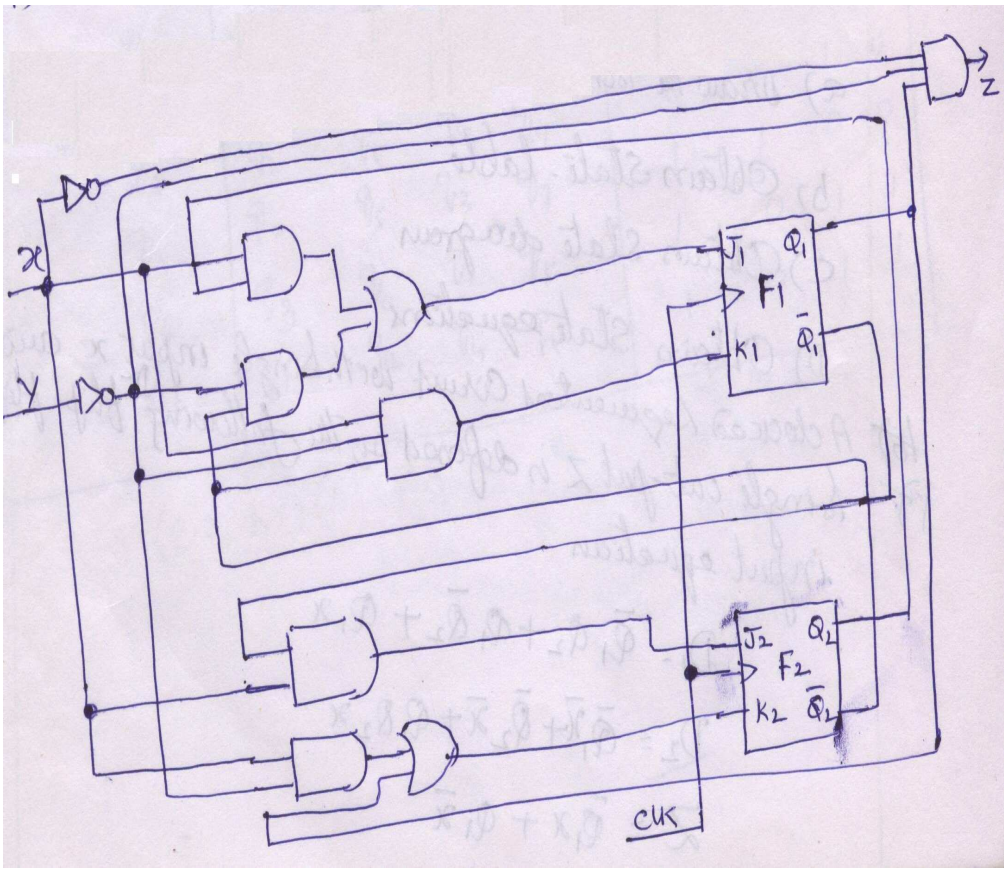

Figure 7

(a) Obtain input equations.

(b) List the state table

(c) Draw the corresponding state diagram.

(d) Derive state - equations. [4+4+4+4]

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, other wise go to T_3.

(b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

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Code No: R05220403 **Set No. 3**

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1. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows? [4 × 4 = 16]
   (a) 001111101010
   (b) 101110010110
   (c) 101110110100
   (d) 110011010111

2. (a) Convert the following expressions in to sum of products and product of sums [8]
      i. (AB + C) (B + C'D)
      ii. x' + x(x + y')(y + z')
   (b) Obtain the Dual of the following Boolean expressions. [8]
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C')

3. (a) Design a logic circuit Using minimum number of Basic gates for the following Boolean expression.
   $F = (\bar{A}\bar{B}\bar{C}\bar{D}) + (\bar{A}\bar{B}\bar{C}D) + (\bar{A}\bar{B}C\bar{D}) + (\bar{A}\bar{B}CD) + (\bar{A}B\bar{C}\bar{D}) + (\bar{A}B\bar{C}D)$
   $+(\bar{A}BC\bar{D}) + (A\bar{B}\bar{C}D) + (AB\bar{C}\bar{D}) + (AB\bar{C}D) + (ABC\bar{D})$
   (b) Reduce the following expression using Karnaugh map. $(\bar{B}\bar{A} + \bar{A}B + A\bar{B})$
   (c) Find the out put of a four variable K-map, when all the cells are filled with logic LOW. [10+4+2]

4. (a) Implement the following multiple output combinational logic using a 4 line to 16 line Decoder.
   (b) Explain the terms Multiplexing and Demultiplexing.
   $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD$
   $Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + AB\bar{C}D$
   $Y_3 = \bar{A}BCD + ABC\bar{D} + ABCD.$ [10+6]

5. Write a brief note on:

(a) Architecture of PLDS

(b) Capabilities and the limitations of thusold gates. [8+8]

6. (a) Compare synchronous & Asynchronous circuits

(b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

7. A clocked sequential circuit is defined by the following state - table:

(a) Using implication table Obtain equivalence classes.

(b) Design the circuit using D - Flip-Flops. [8+8]

P.S	N.S		Z	
	x=0	x=1	x=0	x=1
0	0	4	1	0
1	0	4	0	0
2	1	5	0	0
3	1	5	0	0
4	2	6	0	1
5	2	6	0	1
6	3	7	0	1
7	3	7	0	1

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, other wise go to T_3.

(b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

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Code No: R05220403 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

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1. Convert the following to Decimal and then to Hexadecimal.
   (a) 1234_8
   (b) 1267_8
   (c) 11001111_2
   (d) 11011101_2
   (e) 786_{10}
   (f) 555_{10} [3+3+3+3+2+2]

2. (a) Simplify the following Boolean functions. [8]
      i. x'yz + x'yz' + xy'z' + xy'z
      ii. x'yz + xy'z' + xyz + xyz'
      iii. x'z + x'y + xy'z + yz
      iv. x'y'z' + x'yz' + xy'z' + xy'z + xyz'
   (b) Obtain the complement of the following Boolean expressions. [8]
      i. A'C' + ABC + AC'
      ii. (x'y' + z)' + z + xy + wz
      iii. A'B(D' + C'D) + B(A +A'CD)
      iv. (A' + C)(A' + C')(A + B + C'D)

3. Apply Branching method to simplify the following function
   F (A, B, C, D) = $\prod M(0, 1, 4, 5, 9, 11, 13, 15, 16, 17, 25, 27, 28, 29, 31)d(20, 21, 22, 30)$. [16]

4. (a) Realize Full Adder Using two half adders and logic gates.
   (b) Draw the block diagram of BCD adder using two 4-bit parallel binary adders and logic gates. [4+12]

5. (a) Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input.
   (b) Write a brief note on programmable logic devices. [8+8]

6. (a) Design a sequence detector which detects 110010 Implement the sequence detector by using D - type flipflops

(b) Classify the required circuits into synchronous, asynclironus, clockmode, pulse mode with suitable examples. [8+8]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.

   (a) Obtain State - Diagram.

   (b) Also obtain state - Table.

   (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. For the ASM Figure given in 8:

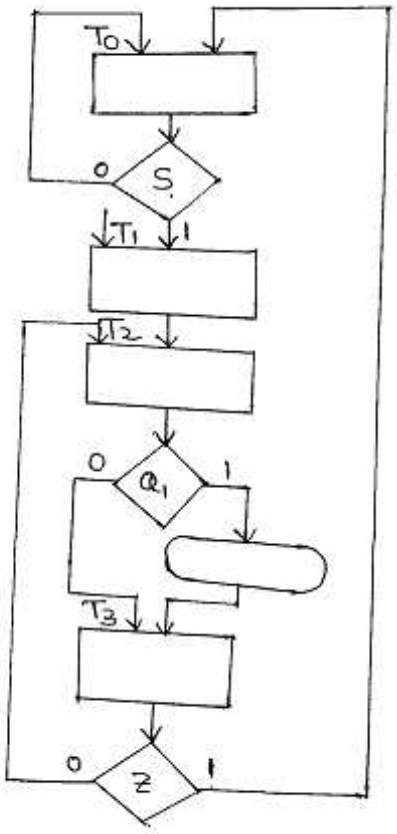

Figure 8

(a) Draw the state diagram.

(b) Design the control unit using D flip-flops and a decoder. [8+8]

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