Set No. 1

II B.Tech I Semester Supplimentary Examinations, February 2008 ELECTRONIC CIRCUIT ANALYSIS (Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks ****

- 1. (a) Using the h-parameter model, derive expressions for current gain, input impedance, voltage gain, and output impedance of a CE amplifier.
 - (b) The h-parameters of a transistor are $h_{fe} = 50$, $h_{ie} = 1.1 \text{K}\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 24 \ \mu\text{A/V}$ Calculate A_I , A_V , A_{VS} , R_i , and R_o . As shown in figure 1b. [8+8]





- 2. (a) Draw the circuit diagram of Darlington pair circuit deriving its important characteristics.
 - (b) For the amplifier shown in figure 2, calculate R_i , $R_I^{'}$, A_V , A_{VS} and $A_I^{'} = -I_2 \ / \ I_1$. The h-parameter values are $h_{fe} = 50, \ h_{ie} = 1.1 \mathrm{K}\Omega, \ h_{re} = 2.5 \mathrm{x} 10^{-4}, \ h_{oe} = 24 \ \mu \mathrm{A/V}.$

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[8]



Figure 2

- 3. (a) Prove that in Hybrid π model, the diffusion capacitance is proportional to the emitter bias current.
 - (b) In Giacolletto model of a transistor at high frequencies, how does C_e vary with $|I_c|$ and $|V_{CE}|$? How does C_c vary with $|I_c|$ and $|V_{CE}|$? [8+8]
- 4. (a) What are the advantages and disadvantages of push pull configuration? Show that in Class-B push pull amplifier the maximum conversion efficiency is 78.5%
 [8]
 - (b) A transistor in a transformer coupled (Class A) power amplifier has to deliver a maximum of 5 Watts to a load of 4Ω load. The quiescent point is adjusted for symmetrical swing, and the collector supply voltage is $V_{CC}=20$ Volts. Assume $V_{min}=0$ volts.
 - i. What is the transformer turns ratio?
 - ii. What is the peak collector current?
- 5. (a) Mention the three methods of stabilization of a single tuned BJT amplifier against the feedback capacitance connected between the base and Collector?
 - (b) Explain in detail various Neutralization techniques with the help of circuit diagrams? [6+10]
- 6. (a) What are the main advantages of class-C operating mode in RF applications?
 - (b) Draw the circuit of class-C radio frequency amplifier and explain its operation with necessary waveforms? [8+8]
- 7. (a) With the help of a neat circuit diagram, explain the operation of BJT shunt voltage regulator.

- (b) What is a voltage reference? Why is it needed?
- (c) What is the function of a series pass transistor? [8+4+4]
- 8. (a) What is catcher diode and explain the necessity of catches diode in Switch Regulator with the help of circuit diagram.
 - (b) List the operating ratings and electrical characteristics of IC 723. [8+8]

Set No. 2

II B.Tech I Semester Supplimentary Examinations, February 2008 ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks

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- 1. (a) Draw the circuit of an Emitter follower and its equivalent circuit. List out its characteristics.
 - (b) Design a single stage Emitter follower having $R_i=500$ K Ω and $R_o=20\Omega$. Assume $h_{fe}=50, h_{ie}=1K, h_{oe}=25\mu$ A/V. [8+8]
- 2. (a) Derive the expression for the low 3-dB frequency f_L^* of n-identical non interacting stages in terms of f_L for one stage.
 - (b) If four identical amplifiers are cascaded each having $f_L = 100$ Hz, determine the overall lower 3dB frequency f_h^* Assume non interacting stages.
 - (c) Write a short note on Gain-Band width product of amplifiers. [5+5+6]
- 3. (a) Draw the small signal equivalent circuit for an emitter follower stage at high frequencies.
 - (b) Consider a CE stage with a resistive load R_L . Using Miller's theorem Find out input capacitance at mid-band frequencies and high frequencies? [8+8]
- 4. (a) Write short notes on requirement and types of heat sinks for power dissipation in large signal amplifiers.
 - (b) With the help of a neat circuit diagram, explain the operation of a complementary symmetry configured class B power amplifier.
 - (c) Compare and contrast push-pull and complementary-symmetry configurations for class B power amplifiers. [6+6+4]
- 5. (a) Why do we use tuned amplifiers in the IF and RF range?
 - (b) Explain in detail how do you alter the bandwidth of an RF amplifier which is
 - i. Single tuned
 - ii. Double tuned
 - iii. Stagger tuned.

- [8+8]
- 6. (a) What is a Video amplifier? Explain the need for video amplifiers?
 - (b) Explain in detail the design considerations of video amplifiers. [6+10]
- 7. (a) Explain the operation of a Zener diode Voltage Regulator.
 - (b) Discuss about the stability factor of a zener diode voltage regulator



- (c) Explain how overload protection is provided in Series Voltage Regulators. $[6{+}4{+}6]$
- 8. (a) What is catcher diode and explain the necessity of catches diode in Switch Regulator with the help of circuit diagram.
 - (b) List the operating ratings and electrical characteristics of IC 723. [8+8]

Set No. 3

II B.Tech I Semester Supplimentary Examinations, February 2008 ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks ****

- 1. (a) Draw the circuit diagram and low frequency equivalent circuit of common source amplifier and derive an expression for its voltage gain.
 - (b) For the emitter follower circuit with $R_S = 0.5$ K and $R_L = 5$ K, calculate A_I, R_i, A_V, A_{VS} , and R_0 . Assume, $h_{fe} = 50$, $h_{ie} = 1$ K, $h_{oe} = 25 \ \mu$ A/V. [8+8]
- 2. (a) Discuss about different types of distortions that occur in amplifier circuits.
 - (b) Three identical non interacting amplifier stages in cascade have an overall gain of 0.3 dB down at 50KHz compared to mid band. Calculate the upper cutoff frequency of the individual stages. [8+8]
- 3. (a) Prove that in Hybrid π model, the diffusion capacitance is proportional to the emitter bias current.
 - (b) In Giacolletto model of a transistor at high frequencies, how does C_e vary with $|I_c|$ and $|V_{CE}|$? How does C_c vary with $|I_c|$ and $|V_{CE}|$? [8+8]
- 4. (a) Classify large signal amplifiers based on its operating point. Distinguish these amplifiers in terms of the conversion efficiency. [8]
 - (b) Draw the push-pull power amplifier circuit. Derive the expression for the output current in push ?pull amplifier with base current as $i_b = I_{bm} \sin wt$. [8]
- 5. Draw the high frequency equivalent circuit of a Tapped single tuned Capacitance coupled amplifier using BJT and derive the expressions for
 - (a) Voltage gain (A)
 - (b) Voltage gain at resonance (A_{res}) [16]
- 6. Explain what you mean by Synchronous tuning of tuned amplifiers? Draw the frequency response of a synchronously tuned amplifier showing the response of individual stages and overall responses? [16]
- 7. (a) The voltage regulator in Figure 7amaintains an output voltage of 25 V.
 - i. What value of Rsc should be used to limit the maximum current to 0.5A?
 - ii. With the value of Rsc found in (i) what will be the output voltage when RL= 100 ohms? When RL =10 ohms?





Figure 7a

- (b) Draw and explain the regulator which will provide the foldback limiting .[8+8]
- 8. (a) Using three pin voltage regulator, design a current source that will deliver 0.25A current to 48 ohms 10W load. From data sheet $I_Q = 4.2$ mA and $V_R = 5$ V [6]
 - (b) Compare IC 723 and IC78XX Voltage Regulators [4]
 - (c) What is UPS and explain how it differs from regulated power supply? [6]

Set No. 4

II B.Tech I Semester Supplimentary Examinations, February 2008 ELECTRONIC CIRCUIT ANALYSIS

(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions All Questions carry equal marks ****

- 1. (a) For a single stage transistor amplifier, $R_S = 10$ K and $R_L = 10$ K. The h-parameter values are $h_{fc} = -51$, $h_{ic} = 1.1$ K Ω , $h_{rc} \approx 1$, $h_{oc} = 25 \mu$ A/V. Find A_I , A_V , A_{VS} , R_i , and R_o for the CC transistor configuration.
 - (b) For a single stage transistor amplifier, $R_S = 5$ K and $R_L = 10$ K The h-parameter values are $h_{fe} = 50$, $h_{ie} = 1.1$ K Ω , $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 25 \ \mu$ A/V. Find A_I, A_V, A_{VS}, R_i , and R_o for the CE transistor configuration. [8+8]
- 2. A two-stage amplifier circuit (CE-CC configuration) is shown in figure 2. The hparameter values are $h_{fe} = 50$, $h_{ie}=2 \text{ K } \Omega$, $h_{re} = 6 \times 10^{-4}$, $h_{oe} = 25 \mu \text{ A/V}$. $h_{fc} = -51$, $h_{ic} = 2 \text{ K} \Omega$, $h_{rc} = 1$, $h_oc = 25 \mu \text{ A/V}$.

Find the input and output impedances and individual, as well as overall voltage and current gains.



Figure 2

- 3. (a) Derive the transfer function of a single stage CE transistor amplifier response.
 - (b) Discuss Miller's Theorem? Apply this theorem to find approximate equivalent circuit for a transistor amplifier stage in CE configuration with a resistive load and hence prove that the voltage with resistive load is $-g_m R_L$. [8+8]
- 4. (a) Draw the circuit of class -A transformer fed power amplifier and derive the expression for output power P_o . [10]

Set No. 4

- (b) What is cross over distortion? How can a Class-AB power amplifier avoid cross-over distortion? [6]
- 5. Draw the High frequency equivalent circuit of a Single tuned Capacitive coupled BJT amplifier and derive the expression for
 - (a) Voltage gain (A)
 - (b) Voltage gain at resonance (A_{res})
 - (c) 3 dB bandwidth.

- [16]
- 6. Explain as to how you can increase the selectivity of single tuned amplifier. Draw the circuit diagram and explain its operation and also draw its frequency response?
 [16]
- 7. (a) The voltage regulator in Figure 7amaintains an output voltage of 25 V.
 - i. What value of Rsc should be used to limit the maximum current to 0.5A?
 - ii. With the value of Rsc found in (i) what will be the output voltage when RL= 100 ohms? When RL =10 ohms?



Figure 7a

- (b) Draw and explain the regulator which will provide the foldback limiting [8+8]
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