Prasad V. Potluri Siddhartha Institute of Technology, Kanuru, Vijayawada.

1/2 M.Tech. FIRST SEMESTER

CSCS1T3 COMPUTER ORGANIZATION AND ARCHITECTURE Credits: 4

Lecture: 4 periods/week Internal assessment: 30 marks

Tutorial: 1 period /week Semester end examination: 70 marks

Objectives:

1. To have a thorough understanding of the basic structure and operation of a digital computer.
2. To have a thorough understanding of computer arithmetic, Boolean algebra, Combinational and Sequential Circuits
3. To study the hierarchical memory system including cache memories and virtual Memory.
4. To study the different ways of communicating with I/O devices and standard I/O interfaces.
5. To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
6. To have a thorough understanding of the central processing unit and various instructions formats together with a variety of addressing modes.
7. To study the concept of pipelining and the way it can speed up the processing, Instruction pipelines and RISC pipelining.
8. To study the issues involved in multiple processor and vector processing organizations.

Learning Outcomes:

Students will have thorough knowledge about

1. Basic structure of a digital computer, the central processing unit and various instruction formats together with a variety of addressing modes.
2. The organization of the Control unit, Arithmetic and Logical unit, Memory unit and the I/O Unit.
3. Instruction pipelining mechanism.
4. Reduced instruction set computer.
5. The issues involved in multiple processor and vector processing organizations.

UNIT - I

Computer Arithmetic and Boolean Algebra: Signed and Unsigned numbers Addition, Subtraction, Multiplication and Division. Floating Point Representation, Floating Point Arithmetic, Logical Gates, Boolean Algebra and simplification of Boolean expressions

UNIT - II

Combinational and Sequential Circuits: Flip-flops, Decoders, Encoders, Multiplexers, Half and Full Adders, Shift Registers, Binary Counters, BCD Adders.

UNIT - III

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory.

UNIT - IV

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupts, DMA, Input-Output Processor, Serial Communication.

UNIT - V

Arithmetic Operations – Algorithms: Signed and Unsigned Numbers: Addition, Subtraction, Multiplication and Division Algorithms.

UNIT - VI

Instruction Sets, Processor Structure and Functions: Addressing, x86 Addressing modes, Instructor Formats, x86 Instruction Formats, Processor Organization, Register Organization, Instruction Cycle, Instruction Pipelining, x86 Processor family.

UNIT - VII

Reduced Instruction Set Computers (RISCs): Instruction Execution Characteristics, Use of Large Register File, Compiler-based Register Optimization, Reduced Instruction Set Architecture, RISC Pipelining, RISC Vs CISC.

UNIT - VIII

Parallel Processing and Multicore Computers: The use of Multiple Processors, Symmetric Multiprocessors, Cache Coherence and the MESI Protocol, Multithreading and Chip Multiprocessors, Clusters, Nonuniform Memory Access Computers, Vector Computation, Multicore Computers: Hardware and Software Performance Issues, Multicore Organization, Intel x86 Multicore Organization.

Learning Resources

Text Books:

1. Computer System Architecture, Morris Mono, 3rd Edition, Pearson/ PHI.
2. Computer Organization and Architecture, William Stallings, 8th Edition, Pearson.

Reference Books:

1. Computer Organization, Hamacher and Vranesic, 5th Edition, TMH.
2. Digital Logic and Computer Organization, Rajaraman and Radha Krishnan, PHI.
3. Micro Computer Systems: 8086 / 8088 Family, Liu and Gibson, 2nd Edition, PHI.