

4/4 B.Tech. SECOND SEMESTER

E85T4D

VLSI DESIGN (ELECTIVE – IV)

Credits: 4

Lecture: 4 periods/week

Internal assessment: 30 marks

Tutorial: 1 period /week

Semester end examination: 70 marks

Course Objectives:

- Understand VLSI Design Flow
- Learn Transistor-Level CMOS Logic Design
- Understand VLSI Fabrication
- Learn to Analyze Gate Function and Timing Characteristics

Learning Outcomes:

- Gain knowledge of different VLSI fabrication processes and CMOS Logic Design.
- Design different MOS logical circuits.
- Understand the effects of Scaling.
- Understand the programmable architectures such as, PLDs, CPLDs and FPGAs.

Unit I Introduction:

Introduction to IC Technology, The IC Era, MOS and related VLSI Technology, Basic MOS Transistors. Enhancement and Depletion modes of transistor action, IC production process. MOS and CMOS Fabrication processes, BiCMOS Technology, Comparison between CMOS and Bipolar technologies.

Unit II Basic Electrical Properties Of Mos And Bicmos Circuits

I_d versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Transconductance and Output Conductance, MOS transistor Figure of Merit, The Pass transistor. The nMOS Inverter, Determination of Pull-up to Pull-Down Ratio for nMOS inverter driven by another nMOS inverter and for an nMOS inverter driven through one or more pass transistors, Alternative forms of pull-up, The CMOS Inverter, MOS transistor circuit model, Bi-CMOS Inverter, Latch-up in CMOS circuits and BiCMOS Latch-up Susceptibility.

Unit III Mos And Bicmos Circuit Design Processes

MOS Layers, Stick Diagrams, Design Rules and Layout, General observations on the Design rules, Layout Diagrams of NAND, NOR gates, CMOS inverter and different logic functions.

Unit IV Basic Circuit Concepts

Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, Some area Capacitance Calculations, The Delay Unit Inverter Delays, Driving large capacitive loads, Propagation Delays, Wiring Capacitances, Fan-in and fan-out characteristics, Choice of layers, Transistor switches, Realization of gates using nMOS, pMOS and CMOS technologies.

Unit V Scaling Of Mos Circuits

Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise, Limits due to current density, Introduction to Switch Logic and Gate Logic

Unit VI Semiconductor Integrated Circuit Design

Introduction to Programmable Logic Devices (PLDs), Programmable Logic Arrays (PLA), Programmable Array Logic (PAL). Implementation approaches in VLSI Design- full Custom Design, Semicustom Design, Gate Arrays, and Standard Cells.

Unit VII Field Programmable Gate Arrays and Complex Programmable Logic Devices

Xilinx 3000 Series FPGAs, Xilinx 4000 Series FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs

Unit VIII Test Principles

Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques, System-level Test Techniques, Layout Design for improved Testability.

Learning resources

Text books:

1. Essentials of VLSI Circuits and Systems- Kamran Eshraghian ,Douglas and A Pucknell, Prentice-Hall of India Private Limited, 2005 Edition .
2. Principles of CMOS VLSI Design - Weste and Eshraghian, Pearson Education, 1999.

Reference books:

1. Chip Design for Submicron VLSI: CMOS Layout & Simulation, - John P. Uyemura, Thomson Learning.
2. Introduction to VLSI Circuits and Systems - John .P. Uyemura, JohnWiley, 2003.
3. Digital Integrated Circuits - John M. Rabaey, PHI, EEE, 1997.
4. Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.
5. VLSI Technology – S.M. SZE, 2nd Edition, TMH, 2003.
6. Fundamentals of Logic Design with VHDL– Stephen. Brown and Zvonko Vranesic, TMH,2005.