4/4 B.Tech - SEVENTH SEMESTER

EC7T5A **Advanced VLSI Design** **Credits: 4**

Lecture : 4 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks** -------
---

Course Objectives:

- Learn the design of high performance CMOS systems.
- Knowledge of non-silicon technologies like GaAs.
- To study different types of memories.
- To study about arithmetic building blocks.

Learning Outcomes:

- Ability to analyze and design static inverters and combinatorial logic gates to determine and meet static & dynamic characteristics and specifications.
- Ability to design and analyze dynamic combinatorial logic gates.
- Ability to design a VLSI subsystem (e.g., adder, shifter, multiplier and decoder) to meet performance specifications.
- Understand memory cell structures and fabrication technologies.

UNIT- I

CMOS inverter: Static CMOS inverter, evaluating the robustness of CMOS inverter, performance of CMOS inverter, power consumption and power delay product and pass transistor logic.

UNIT- II

High performance digital circuits: Emitter coupled logic(ECL),Differential ECL, ECL with active pull downs, ECL logic families, BiCMOS logic, GaAs devices and their properties and GaAs digital circuit design.

UNIT- III

Dynamic logic circuits: Dynamic CMOS logic(Precharge –Evaluate logic), noise considerations in dynamic logic, cascading dynamic gates, Domino CMOS logic, Pseudo static latch,C^2 MOS latch, NORA – CMOS logic, true single phase clocked logic(TSPCL).

UNIT- IV

Arithmetic building blocks I: Barrel shifter , logarithmic shifter , ripple carry adder, carry look ahead adder, carry select adder ,carry bypass adder, Manchester carry chain adder, carry save adder, Parity generators, Comparators, Zero/One Detectors.

UNIT- V

Arithmetic building blocks II: Array multiplier, Baugh Wooley multiplier , Booth multiplier and Wallace tree multiplier.

UNIT- VI

Memory Elements: ROM, PROM, EPROM, EEPROM, SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar. DRAM and timing parameters of DRAM, SDRAM and DDRSDRAM.

UNIT- VII

Design Methodologies: Design verification, electrical verification, Timing verification, functional verification, circuit synthesis, logic synthesis, architecture synthesis, custom circuit design, cell based design and array based design.

UNIT- VIII

Digital Design with SM Charts : State Machine Charts, Derivation of SM Charts, Realization of SM Charts, Implementation of SM chart for multiplier.

Learning Resources

Text Books:

1. Digital Integrated Circuits, Jan M. Rabaey, Anantha P. Chandrakasan, Borivoje Nikolić,Pearson Education, 2003.
2. CMOS Digital Integrated Circuits - Analysis & Design, Sung-Mo Kang & Yusuf Leblebici, Mc Graw Hill, 3rd Edition, 2002.

References:

1. Introduction to VLSI Circuits and systems, John P. Uyemura, John Wiley & sons, 2002.
2. VLSI-Design of Non-Volatile Memories, **Campardo**, Giovanni, **Micheloni**, Rino**, Novosel,** David, Springer, 2005.
3. Fundamentals of Logic Design with VHDL– Stephen. Brown and Zvonko Vranesic, TMH, 2005.