3/4 B.Tech - FIFTH SEMESTER

EC5T1 Computer Architecture & Organization Credits: 4

Lecture : 4 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks** -------
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Course Objectives:

- To have a thorough understanding of the basic structure and operation of a digital computer.
- To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
- To study the different ways of communicating with I/O devices and standard I/O interfaces, pipeline and vector processing.
- To study the hierarchical memory system including cache memories and virtual memory.

Learning Outcomes:

- Understand the merits and pitfalls in computer performance measurements.
- Understand the impact of instruction set architecture on cost-performance of computer design.
- Design a pipeline for consistent execution of instructions with minimum hazards.
- Understand ways to incorporate long latency operations in pipeline design.
- Understand ways to take advantage of instruction level parallelism for high performance design.
- Understand dynamic scheduling methods and their adaptation to contemporary microprocessor design.
- Understand the impact of branch scheduling techniques and their impact on processor performance.
- Understand alternatives in cache design and their impacts on cost/performance.

UNIT-I

Register Transfer and Microoperations: Register Transfer Language, Register Transfer, Bus and Memory Transfers, Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift unit

UNIT-II

Basic Computer Organization and Design: Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction cycle. Memory Reference Instructions. Input-Output and Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator Logic.

UNIT-III

Microprogrammed Control: Control Memory, Address Sequencing, Microprogram Example, Design of control unit.

UNIT-IV

Central Processing Unit: Introduction, General Register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation Program control, Reduced Instruction Set Computer (RISC), Overlapped Register Windows

UNIT-V

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access(DMA), Input- Output Processor(IOP), Serial Communication

UNIT-VI

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware

UNIT-VII

Computer Arithmetic: Introduction, Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating-Point Arithmetic Operations, Decimal Arithmetic Unit, Decimal Arithmetic Operations.

UNIT-VIII

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors

Learning Resources

Text Books:

1. Computer System Architecture, M. Moris Mano, Pearson/ PHI, 3rd Edition, 2007
2. Computer Organization and Architecture, William Stallings, PHI/Pearson, 7th Edition 2006.

References:

1. Computer Organization, Car Hamacher, Zvonks Vranesic, Safwat Zaky, 5th Edition, McGrawHill. 2002
2. Computer Architecture and Organization, John P. Hayes., Tata Mc Graw Hill International, 3rd edition,1998.
3. Computer Architecture: A quantitative approach, John L. Hennessy, David A. Patterson,Tata Mc Graw Hill International 4th edition,2006.
4. Structured Computer Organization, Andrew S. Tanenbaum, , Prentice Hall , 4th edition 1998