3/3 MCA First Semester

CA5T4D **ADVANCED COMPUTER ARCHITECTURE** **Credits : 4**

Lecture Hours : 4 periods / week Internal assessment : 30 Marks

Semester and Examination: 70 Marks

Course Description:

This course deals with quantitative approach, the student has to understand the essentials their computer issues. It presents interesting examples of contemporary and important historical Instruction set architecture. RISC architecture-The focus of so much work in the last 20 years is by no means the final word here. And after that it describes Instruction Level Parallelism (ILP): The ability to execute more than one instruction at a time. Some of the techniques are RISC & VLIW computing. But as later chapters here point out, both RISC and especially VLIW as praciticxed in the INTEL Itanium architecture are very power intensive. There is thus a clear counter trend emerging using simpler pipelines with more realistic levels of ILP while exploiting other kinds of parallelism by running both multiple threads of execution per processor and after multiple processors on a single chip.

The challenge for designers of high performance systems of the future is to understand when simultaneous execution is possible, but then to use these technologies judicially in combination with other, less granular techniques that are less power intensive and complex. The classical design of cache, main memory hierarchies and virtual memory. And it will deals with thread level parallelism.

Course Objective:

- Extrapolate the performance and price-performance measurements of processors designed for the desktop, server and embedded markets, as well as consider the power efficiency of embedded processor.
- Summarize how the structure of modern compilers affect the utility of instruction sets for traditional computers, DSPs and media extensions.
- Identify the central issues of various hardware based approaches to exploit Instruction Level Parallelism(ILP).
- Identify the central issues of various software based approaches to exploit Instruction Level Parallelism(ILP).

UNIT I:

Fundamentals of Computer design: Technology trends- cost- measuring and reporting performance quantitative principles of computer design.

UNIT II:

Instruction set principles and examples: classifying instruction set-memory addressing- type and size of operands- addressing modes for signal processing-operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler.

UNIT III:

Instruction level parallelism (ILP): over coming data hazards- reducing branch costs –high performance instruction delivery- hardware based speculation- limitation of ILP.

UNIT IV:

Approaches & Protections: ILP software approach - compiler techniques-static branch protection - VLIW approach - H.W support for more ILP at compile time- H.W verses S.W Solutions.

UNIT V:

Memory hierarchy design: cache performance- reducing cache misses penalty and miss rate – virtual memory- protection and examples of VM.

UNIT VI:

Multiprocessors and thread level parallelism: symmetric shared memory architectures - distributed shared memory- Synchronization- multi threading.

UNIT VII:

Storage systems: Types – Buses - RAID- errors and failures- bench marking a storage device- designing a I/O system.

UNIT VIII:

Inter connection networks and clusters: interconnection network media – practical issues in interconnecting networks- examples – clusters-designing a cluster.

Learning Resources

Text Books:

1. Computer Architecture A quantitative approach, John L. Hennessy & David A. Patterson Morgan Kufmann (An Imprint of Elsevier), 3/e, 2003

Reference Books:

1. "Computer Architecture and parallel Processing" Kai Hwang and A.Briggs International Edition McGraw-Hill, 1984.
2. Advanced Computer Architectures, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson, 1997.
3. Parallel Computer Architecture, A Hardware / Software Approach, David E. Culler, Jaswinder Pal singh with Anoop Gupta, Elsevier, 1999.