PVP-19

DIGITAL INTEGRATED CIRCUITS DESIGN

Course Code	19EC4701C	**Year**	IV	**Semester**	I
Course Category	Program Elective-IV	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Digital Logic Design
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Design CMOS inverters (L5)
CO2	Analyze different scaling methods for MOS logical circuits (L4)
CO3	Implement different techniques to improve Area, power and speed of MOS logical circuits (L3).
CO4	Analyze timing issues and arithmetic building blocks . (L4)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	3		3		3					3			3	
CO2	3		3		3					3			3	
CO3	3	3								3			3	
CO4	3	3								3			3	
Average* (Rounded to nearest integer)	3	3	3	3	3					3			3	

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**CMOS INVERTER:** Introduction, The static CMOS inverter, Evaluating the robustness of CMOS inverter, Performance of CMOS inverter, Dynamic behaviour of CMOS inverter, and Power delay product	CO-1
II	Technology scaling in VLSI, Full Scaling , Constant Voltage scaling , combined(mixed) scaling methods ,scaling factors for MOS circuits: Logic gate Area, gate capacitance, carrier density,, channel resistance, gate delay, maximum operating frequency, saturation current, current density, power dissipation and power –delay product.	CO-2
III	**DESIGNING COMBINATIONAL LOGIC GATES IN CMOS:** Ratioed Logic , Pass transistor Logic, Static CMOS design, Dynamic Domino CMOS logic design, performance of Dynamic logic, switching activity of logic gate, short circuit currents in CMOS logic gates, Power Consumption in CMOS Gates, Designing BICMOS logic gates	CO-3

IV	**TIMING ISSUES IN DIGITAL CIRCUITS**: Introduction, Timing classification of digital systems, Synchronous design, Clock Skew and Clock Generation. Synchronization at the system level, synchronous verses asynchronous design	CO-4
V	**DESIGNING ARITHMETIC BUILDING BLOCKS**: Data paths in Digital processor architectures, carry select adder, Carry Skip Adder ,Carry Look Ahead Adder , Carry Save Adder , multiplier, shifter, Power and speed trade-offs in data path structures	CO-4

Learning Resources
Text Books
1. Digital Integrated Circuits- Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Second Edition, PHI.
Reference Books
1. CMOS VLSI Design- Neil H.E.Weste, David Money Harris, Fourth Edition

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