4/4 B.Tech - SEVENTH SEMESTER

EC7T4B **DSP Processors and Architectures** **Credits: 4**

Lecture : 4 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks**

Course Objectives:

- The purpose of this course is to introduce the concepts of DSP Processor and its architectures.
- To program DSP Processor for various applications.

UNIT-I

Computational Accuracy in DSP Implementations: Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementations, A/D Conversion Errors, DSP Computational Errors, D/A Conversion Errors.

UNIT-II

Architectures for Programmable DSP Devices: Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

UNIT-III

Execution Control and Pipelining: Hardware Looping, Interrupts, Stacks, Relative Branch Support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching Effects,Interrupt Effects, Pipeline Programming Models.

UNIT-IV

Programmable Digital Signal Processors: Commercial Digital Signal-Processing Devices, Data Addressing Modes of TMS320C54XX DSPs, Data Addressing Modes of TMS320C54XX Processors, Memory Space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-V

Implementations of Basic DSP Algorithms: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT-VI

Implementation of FFT Algorithms: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and Scaling, Bit-Reversed Index Generation, An 8-Point FFT Implementation on the TMS320C54XX, Computation of the Signal Spectrum.VR10 Regulations

UNIT-VII

Interfacing Memory and I/O Peripherals to Programmable DSP devices I: Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts And I/O, Direct Memory Access (DMA).

UNIT-VIII

Interfacing Memory and I/O Peripherals to Programmable DSP Devices -II:A Multi channel Buffered Serial Port (MCBSP), MCBSP Programming, A CODEC Interface Circuit, CODEC Programming, A CODEC-DSP Interface Example.

Learning Resources

Text Books:

1. DSP Processors and Architectures, Avatar Singh and S.Srinivasan, Thomson Publications2004.
2. DSP Processor Fundamentals, Architectures & Feature, , Lapsley et al, S. Chand & Co 2000

References:

1. Digital Signal Processors, Architecture, Programming and Applications, B. Venkataramani and M. Bhaskar, TMH., 2002
2. Digital Signal Processing, Jonatham Stein, John Wiley , 2005